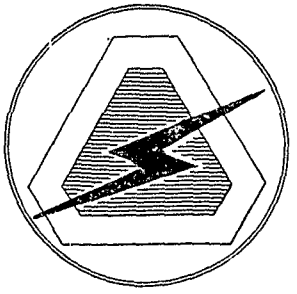
AD 422378

USAELRDL Technical Report 2386

STATIC AND DYNAMIC PERFORMANCE OF MICROPOWER TRANSISTOR LINEAR AMPLIFIERS

R. A. Gilson
O. Pitzalis
W. Kiss
and
J. D. Meindl



September 1963

UNITED STATES ARMY
ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORY
FORT MONMOUTH, N.J.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORIES
FORT MONMOUTH, NEW JERSEY

September 1963

USAELRDL Technical Report 2386 has been prepared under the supervision of the Director, Electronic Components Department, and is published for the information and guidance of all concerned. Suggestions or criticisms relative to the form, contents, purpose, or use of this publication should be referred to the Commanding Officer, U.S. Army Electronics Research and Development Laboratories, Fort Monmouth, New Jersey, Attn: Chief, Semiconductor and Microelectronics Branch, Solid State and Frequency Control Division.

J. M. KIMBROUGH, JR.
Colonel, Signal Corps
Commanding

OFFICIAL:
B. B. PALMER
Major, WAC
Adjutant

DISTRIBUTION:
Special

STATIC AND DYNAMIC PERFORMANCE OF MICROPOWER TRANSISTOR LINEAR AMPLIFIERS

R. A. Gilson, O. Pitzalis, W. Kiss and J. D. Meindl

DA TASK #1G622001A05602

ABSTRACT

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micropower amplifier. Subject to initial constraints, the design technique: (1) provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and (3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of 5×10^4 ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100^{\circ}C$ for a power drain of 23×10^{-6} w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

U. S. ARMY ELECTRONICS RESEARCH AND DEVELOPMENT LABORATORIES
FORT MONMOUTH, NEW JERSEY

CONTENTS

CONTENTS

STATIC AND DYNAMIC PERFORMANCE OF MICROPOWER TRANSISTOR LINEAR AMPLIFIERS

INTRODUCTION

Recent advances in semiconductor device technology have produced silicon planar transistors which exhibit junction reverse currents less than one nanoampere and common emitter current gains greater than 50 for collector currents of 1 to 10 microamperes. This collector current range is about three orders of magnitude smaller than the normal milliampere operating current range for low power silicon transistors. Because of their ultra low level operational capabilities, "micropower" transistors are of general interest in microelectronics and among their possible applications offer a potential solution to the troublesome problem of battery power drain in portable military communications equipment. The purpose of this report is to describe the results of a feasibility study of the application of micropower transistors in linear communications circuits.

The discussion is divided into three sections. The first section describes the salient characteristics of micropower transistors for the common emitter mode, including the static base and collector characteristics and the small signal fourpole parameters and equivalent circuit. The second section describes an optimum design theory for linear broadband micropower amplifiers which provides a unified and worst case treatment of the DC and large signal AC design of an amplifier, an analysis of small signal behavior, and an AC temperature compensation technique. A linear broadband amplifier is considered since it is the most widely encountered generic communications circuit. The third section of the discussion describes the overall performance of broadband micropower amplifiers, including their effective large signal mode of operation, frequency response, temperature behavior and the influence of key design parameters on amplifier performance.

SECTION 1 - TRANSISTOR CHARACTERIZATION

The purpose of this section is to present characterization data for six typical diffused silicon micropower transistors providing useful information for device applications in linear communications circuits. The devices described include three NPN planar transistors (devices, A, B, and C), an NPN planar epitaxial transistor (device D), an NPN mesa transistor (device E), and a PNP planar transistor (device F) each of which is supplied by a different manufacturer. In Part 1 of the section, the static transistor characteristics are reviewed, and in Part 2 the small signal AC characteristics are considered.

Part 1 - DC Characteristics

Figure 1 displays collector characteristic curves for a typical micropower device for representative operating conditions in the common emitter configuration. In their general appearance, these collector characteristics closely resemble the familiar transistor behavior for the milliampere range of operation. Although not strikingly displayed by the curves of Figure 1, two mild departures from milliampere characteristics are the lower saturation voltage and the lack of the usual flatness in the active region. In addition, the current transfer characteristics, I_C versus I_B curves with V_{CE} held constant, are relatively nonlinear due to the rapid increase of h_{FE} with I_C in the microampere range.

Figure 2 displays typical base-emitter characteristics for the micropower range. It is evident that the general features of the input behavior are similar to those of the normal milliampere collector current range. In essence, Figure 2 illustrates the reason micropower device voltage levels cannot be materially reduced below normal device voltages, although current levels are 10^3 times smaller. The familiar exponential relationship[1] between current and voltage for a semiconductor junction:

$$I = I_s \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \qquad (1.01)$$

where I_s = junction reverse saturation current; q = electronic charge = 1.60×10^{-19} coulombs, k = Boltzmann's constant = 1.38×10^{-23} joules/°K and T = temperature in °K, permits orders of magnitude change in junction current I for small percentage changes in applied voltage V.

At room temperature junction reverse currents below one nanoampere are common for low power silicon planar transistors. Many devices can be found which exhibit a collector-to-base leakage current I_{CBO} less than 0.1 microampere at 150°C. However, at this time the majority of commercial specifications for micropower transistors quote a maximum value for I_{CBO} at 150°C in excess of 1.0 μa for collector voltages of 40 v or more. In these

devices at temperatures above 100°C, I_{CBO} can become significant compared to base current I_B, if not collector current I_C, for collector currents in the 1 to 10μa range. Conservative design practice requires that I_{CBO} be considered in the design of the base bias network for a high temperature micropower amplifier.

A typical characteristic of silicon micropower transistors is a common emitter current gain h_{FE} which is more temperature sensitive for collector currents of 1 to 10μa than for 1 to 10 ma collector currents. Figure 3 shows the temperature variation of h_{FE} for $I_C = 10\mu a$, corrected for I_{CBO}, for a typical silicon micropower transistor. Here it is evident that more than a four-time increase in h_{FE} for $-50 \leq T \leq 100°C$ occurs where at $I_C = 1.0$ ma a three-to-one variation is more typical. This enlarged variation of h_{FE} can be attributed to a shift with current level in the relative importance of the various mechanisms which contribute to the base current in a silicon planar transistor. At low current levels the base current is dominated by surface currents which originate at the surface edge of the emitter[2].

The maximum allowable device power dissipation and breakdown voltages for micropower transistors are far in excess of the requirements of typical micropower amplifiers. Maximum device ratings are generally of small concern in micropower circuits. Table I shows a summary of the salient DC characteristics of devices A through F.

Part 2 - AC Characteristics

The variations with collector current of the small-signal low-frequency common emitter fourpole parameters, $h_{11e} = h_{ie}$ and $h_{21e} = h_{fe}$, of a typical micropower transistor are shown by Figure 4. These measurements clearly indicate the drastic changes which occur in the values of the input impedance h_{11e} and forward current transfer ratio h_{21e} as quiescent collector current is reduced. Table I indicates the marked temperature behavior of the micropower parameters h_{11e} and h_{21e}. Typical values for the reverse voltage transfer ratio $h_{12e} = h_{re}$ and the output admittance $h_{22e} = h_{oe}$ for micropower transistors are indicated at the bottom of Table I; h_{12e} and h_{22e} can generally be neglected in linear micropower circuit analysis.

The frequency behavior of a micropower transistor for the common emitter mode is most conveniently described by the hybrid pi equivalent circuit. However, the frequency behavior of the forward current transfer ratio or current gain h_{21e} is often of special interest. A typical family of measured frequency response curves for h_{21e} is illustrated in Figure 5. The familiar 6 db/octave roll-off is evident. In addition, it is apparent that the gain-bandwidth product for this typical device increases directly with collector current. Table I gives additional data on the frequency behavior of h_{21e} in terms of f_{3db} and f_T.

The common emitter hybrid pi equivalent circuit[3] for a micropower transistor is shown in Figure 6. From an ultra-high frequency immittance bridge measurement, the base spreading resistance of a typical micropower device is $r_{b'} \simeq 50\Omega$ and does not vary significantly for $10\mu a \leq I_C \leq 1.0$ ma. From audio frequency voltage measurements at room temperature, the common emitter diffusion resistance $r_{b'e} \simeq h_{11e} \simeq 200,000\Omega$ for $I_C \simeq 10\mu a$. The calculated value is

(1.02)

$$r_{b'e} = r_{b'} + \frac{r_\epsilon}{1-\alpha_o} \simeq h_{fe} \quad r_\epsilon = h_{fe}\frac{kT}{qI_E} = h_{fe}\frac{0.026}{I_E} = 192,000\Omega$$

where $\alpha_o \simeq h_{fb} = h_{21b}$ is the common base small-signal low-frequency current gain, $r_\epsilon \simeq h_{ib}$ is the common base diffusion resistance, T = 300°K and $I_C \simeq I_E = 10\mu a$. The base-to-emitter capacitance $C_{b'e}$ is composed of the diffusion capacitance C_D and the emitter barrier capacitance C_{Te}. That is

$$C_{b'e} = C_D + C_{Te} \tag{1.03}$$

where for homogeneous base transistors

$$C_D = \frac{qI_E}{kT}\frac{W^2}{2D} \tag{1.04}$$

where W = the electrical base width and D = the minority carrier diffusion constant. For graded base devices C_D is also directly proportional to I_E. From high-frequency capacitance bridge measurements, the diffusion capacitance for a typical micropower transistor was measured as $C_D \simeq 27.2$ picofarads for I_C = 1.0 ma. Therefore, on the basis of (1.04) one would predict C_D = 0.272 pf for $I_C = 10\mu a$. The typical curves of junction capacitance versus voltage given by Figure 7 indicate that $C_{Te} \geq 20$ pf for a forward base bias which produces $I_C = 10\mu a$. Here it is obvious that the diffusion capacitance C_D is apparently much less than the emitter barrier capacitance C_{Te}. C_D may be neglected in the micropower transistor equivalent circuit with no significant loss of accuracy for collector currents less than about $10\mu a$. The data of Table I provide further support for this simplification. The collector capacitance C_C is composed virtually entirely of the collector junction capacitance with a negligible contribution from collector diffusion capacitance. Figure 7 indicates the typical variations of the emitter junction capacitance C_{Te} as well as C_C with applied bias voltage and temperature. The collector current generator has the usual value:

$$g_m v_{b'e} = \frac{\alpha_o}{r_\epsilon} v_{b'e} \quad . \tag{1.05}$$

As a check on the accuracy of the proposed equivalent circuit, one may calculate from Figure 6:

$$h_{fe}(\omega) \simeq \frac{\alpha_o / 1-\alpha_o}{1+j\omega\, r_{b'e}\left[C_{Te}+C_C+C_s\right]} \qquad (1.06)$$

and for the cut-off frequency

$$f_{3db} \simeq \frac{1}{2\pi\, r_{b'e}(C_{Te}+C_C+C_s)} \qquad (1.07)$$

where C_s represents 0.70 pf of transistor stray capacitance including 0.10 pf of stray base-to-emitter header capacitance and 0.60 pf stray collector-to-base header capacitance. For $I_c = 10\mu a$, $r_{b'e} = 200,000\Omega$, $C_{Te} = 22$ pf and $C_C = 7$ pf (1.07) gives $f_{3db} = 26.8$ KC. This compares favorably with the measured value of 25 KC, corrected for stray jig capacitance, given by Figure 5. In many applications, the equivalent circuit of Figure 6 may be simplified by neglecting the base spreading resistance $r_{b'} \simeq 50\Omega$ since $r_{b'} < < r_{b'e} \geq 200,000\Omega$ for $I_c \leq 10\mu a$ and $r_{b'} << \left| j\omega C_{Te} \right| \geq 500\Omega$ for $f \leq 10$ MC. A common figure of merit for a transistor is the gain-bandwidth product given by:

$$\omega_T = h_{fe}\omega_{3db} = \frac{\alpha_o}{1-\alpha_o} \frac{1}{r_{b'e}(C_{Te}+C_C+C_s)} \simeq \left(\frac{q}{kT}\right) \frac{I_C}{(C_{Te}+C_C+C_s)} \,. \qquad (1.08)$$

From (1.08) it is evident that power dissipation may be traded for gain-bandwidth product by increasing I_C. In addition, the transistor barrier capacitances, C_{Te} and C_C, and stray capacitance C_s should be as small as possible for a large gain-bandwidth product. The capacitance of a linearly graded junction may be expressed as

$$C = A\left[\frac{qa\epsilon^2}{12\left|v\right|}\right]^{1/3} \qquad (1.09)$$

where A is the junction area, q is the electronic charge, a is the slope of the linear impurity gradient, ϵ is the material dielectric constant and $\left|v\right|$ is the absolute magnitude of the sum of the junction equilibrium potential difference and the applied voltage. Here it is evident that q is a fundamental constant, ϵ is a material constant, v is virtually constant as described in connection with (1.01) and that allowable decreases in a are largely ineffective in reducing C. Obviously, the principal path open to reducing junction barrier capacitance C, in order to increase the gain-bandwidth product of micropower transistors, is to reduce junction area A. For a given I_C, this of course entails an increase in the current density in the device.

SECTION 2 - DESIGN THEORY

The schematic diagram of a typical broadband micropower amplifier is shown in Figure 8. Among the more common constraints which must be observed in the design of this amplifier are: 1) The supply voltage V_{CC} is fixed. 2) The load impedance R_L is specified. 3) The peak AC output voltage V_L is specified. 4) The operating temperature range $T_Y \leq T \leq T_X$ is fixed. 5) The DC power consumption of the amplifier P_D should be as small as possible. 6) The amplifier bandwidth ω_{3db} is specified. Assuming the foregoing constraints on the design of a micropower amplifier, several problems arise which are far less severe or even nonexistent at normal milliwatt power levels in silicon transistor linear circuits. With regard to DC operation, transistor bias point stabilization becomes more difficult due to three factors: 1) At 1 to 10 microampere collector currents, collector junction reverse current I_{CBO} can become significant at temperatures above 100°C. 2) The temperature variation of common emitter current gain h_{FE} is comparatively large; a five-to-one variation for $-50°C \leq T \leq 100°C$ is not unusual. 3) The effect of the temperature variation of base-emitter diode conductance g_{BE} becomes more difficult to counteract at the low battery voltages which usually accompany microwatt power levels.

With regard to AC operation, a major concern derives from the fact that microampere quiescent collector currents severely restrict the dynamic range of an amplifier and effectively contribute to a large-signal mode of operation. In this connection careful attention must be paid to the effects of temperature as well as saturation and cut-off on the dynamic range of a design. The influence of both transistor and passive component tolerances assumes a greater importance in micropower amplifiers, particularly in view of constraints 3) and 5). The lack of high-frequency response of currently available silicon transistors at microwatt power levels seriously limits the bandwidth of micropower amplifiers. Finally, the relatively large temperature variation of the AC parameters of a micropower transistor tends to limit the AC temperature stability of micropower amplifiers. This section outlines a design theory which has been found useful in deriving micropower amplifier designs which adequately satisfy the previously listed constraints. The section is divided into six parts which present the rudiments of the design technique in Part 1, the cut-off and saturation off-set refinements and the feedback refinement in Part 2, the worst case tolerance refinement in Part 3, an analysis of amplifier small-signal AC characteristics in Part 4, an AC temperature compensation technique in Part 5, and the design and analysis of a cascode circuit with improved frequency response in Part 6.

Part 1 - Basic Design Theory

The DC load line (DC LL) of the micropower amplifier of Figure 8 is given by

$$V_{CC} = I_{Cn} R_C + V_{CEn} + V_{R1n} \qquad (2.01)$$

at a nominal temperature T_n where $V_{R1n} = I_{En}R_1 \cong I_{Cn}R_1$. In order to provide the specified peak AC output voltage V_L at T_n for a minimum DC power dissipation, the amplifier output leg must be designed so that the DC operating point Q_n bisects the AC load line (AC LL) given by

$$I_{Cn} = -(G_C + G_L)\, V_{CEn} \tag{2.02}$$

at T_n for $R_e = 0$. Equation (2.02) represents the AC LL in the DC collector characteristics (I_C, V_{CE}) plane. Although it is properly an AC equation, it is convenient to write it in terms of DC quantities in formulating the design theory. This technique will be used throughout this section.

The locus of all AC load line midpoints is given by [4]

$$I_{Cn} = (G_C + G_L)\, V_{CEn} \quad . \tag{2.03}$$

In (2.02) and (2.03), V_{CEn} must be sufficient to accommodate the specified peak AC output voltage V_L. That is, neglecting for the moment the effects of cut-off and saturation in the transistor

$$V_{CEn} = V_L = I_L/G_L \tag{2.04}$$

where I_L is the peak AC output current. Substituting (2.04) into (2.01) and (2.03) gives

$$I_{Cn} = V_L G_L \, \frac{(V_{CC} - V_L - V_{R1n})}{(V_{CC} - 2V_L - V_{R1n})} \tag{2.05}$$

and

$$R_C = \frac{(V_{CC} - 2V_L - V_{R1n})}{V_L G_L} \quad . \tag{2.06}$$

Given V_{R1n}, equations (2.05) and (2.06) define the smallest I_{Cn} and the largest R_C, respectively, which satisfy the initial design constraints on V_{CC}, R_L and V_L. This is advantageous since small I_C tends to decrease power dissipation P_D and large R_C tends to increase amplifier gain. The proper selection of V_{R1n} in (2.05) and (2.06) obviously constitutes a key point in the design. $V_{R1n} \cong I_{Cn}R_1$ represents the DC feedback voltage which must be used to stabilize the circuit against transistor DC parameter temperature variations for the range $T_y \leq T \leq T_x$. A practical procedure is to compute complete designs for several values of V_{R1n} and then choose the one giving the desired values of AC power gain and DC power dissipation. This procedure will be illustrated in Section 3.

From Figure 9 it is evident that because the quiescent point bisects the AC load line at T_n, operating point drift will limit the output voltage swing to values less than V_L when $T \neq T_n$. A key feature of the present design theory lies in regulating the DC operating point drift such that the desired AC output voltage swings at the operating temperature limits

(i.e., $K_y V_L$ at T_y and $K_x V_L$ at T_x with $0 < K_y, K_x < 1$) are exactly accommodated. From Figure 9, it is apparent that

$$K_y V_L = I_{Cy}/G_C+G_L \text{ or } I_{Cy} = K_y V_L(G_C+G_L) \text{ at } T_y \tag{2.07}$$

and $$K_x V_L = V_{CEx} \text{ at } T_x \quad . \tag{2.08}$$

(By selecting $K_y = K_x = 1/\sqrt{2}$, for example, the AC power output capability of the amplifier will be 3db below its nominal value at the operating temperature limits, T_y and T_x, of the amplifier. It might also be mentioned here that if G_L varies with temperature it should be reflected in the K values which are selected in (2.07) and (2.08).) The output leg DC equation at T_y,

$$V_{CEy} = V_{CC} - I_{Cy}(R_1 + R_C) \tag{2.09}$$

together with (2.07) gives the operating point (I_{Cy}, V_{CEy}) at T_y. The output leg DC equation at T_x,

$$I_{Cx} = \frac{V_{CC} - V_{CEx}}{R_1 + R_C} \tag{2.10}$$

together with (2.08) gives (I_{Cx}, V_{CEx}). It is evident here that the selection of the factors K_y and K_x or the AC dynamic range stability of the amplifier effectively determines its DC operating point stability.

To complete the design, the input leg must be considered. From Figure 8,

$$V_{CC} = (I_B + I_2) R_3 + I_2 R_2 \tag{2.11}$$

and $$0 = V_{BE} + I_E R_1 - I_2 R_2 \quad . \tag{2.12}$$

Writing (2.11) and (2.12) at both the operating temperature limits (T_y and T_x) and solving the four resultant simultaneous equations yields

$$R_2 = \frac{R_3 \left[I_{Ex} R_1 + V_{BEx} \right]}{V_{CC} - I_{Bx} R_3 - V_{BEx} - I_{Ex} R_1} \tag{2.13}$$

and $$R_3 = \frac{V_{CC} \left[(I_{Ex} - I_{Ey}) R_1 - (V_{BEy} - V_{BEx}) \right]}{(I_{Ex} I_{By} - I_{Ey} I_{Bx}) R_1 + (V_{BEx} I_{By} - V_{BEy} I_{Bx})} \quad . \tag{2.14}$$

This procedure for determining R_2 and R_3 yields their largest allowable values for the associated DC operating point stability and emitter resistance R_1[5]. This is accomplished due to the fact that I_{By}, I_{Bx}, V_{BEy} and V_{BEx} in (2.13) and (2.14) effectively take into account the exact overall changes in the transistor parameters I_{CBO}, h_{FE} and g_{BE} for the temperature range $T_y \leq T \leq T_x$. The obvious advantages of large R_2 and R_3 are smaller DC

power dissipation and larger AC power gain for the amplifier. At this point it appears that a rudimentary design theory which satisfies the original constraints on V_{CC}, R_L, V_L, T and P_D has been established.

Part 2 - Saturation, Cut-off and Feedback Refinements

At the relatively low supply and quiescent collector voltage levels associated with battery operated micropower circuits, saturation effects in the transistor may impose a serious limitation on output voltage swing. In addition the monotonic fall-off of current gain h_{FE} with decreasing collector current restricts the AC swing in the low current cut-off region. The distortion caused by these two effects as well as the bandwidth of the amplifier can be improved by providing negative feedback through the emitter resistor R_e (Figure 8). The procedure for quantitative consideration of saturation, cut-off and feedback will now be outlined.

The AC LL equation in the DC collector characteristics plane may be written as

$$V_{CEn} = \frac{-I_{Cn}}{G_C+G_L} - V_{Ren} \qquad (2.15)$$

where V_{Ren} is the AC feedback voltage. Considering feedback only, the locus of AC LL midpoints is given by

$$V_{CEn} = \frac{I_{Cn}}{G_C+G_L} + V_{Ren} \quad . \qquad (2.16)$$

A simple translation of coordinate axes facilitates the desired inclusion of saturation and cut-off effects in (2.16) (see Figure 10).

$$V_{CEn} - V_o = \frac{I_{Cn} - I_o}{G_C + G_L} + V_{Ren} \qquad (2.17)$$

with $V_{Ren} = (I_{En}-I_o)\,R_e \simeq (I_{Cn}-I_o)R_e$ gives the locus of AC LL midpoints considering the saturation V_o and cut-off I_o offsets. The quiescent collector voltage required to accommodate a peak output voltage V_L is

$$V_{CEn} = V_L + V_{Ren} + V_o \quad . \qquad (2.18)$$

Substituting (2.18) into (2.01) and (2.17), one may solve for

$$I_{Cn} = \frac{V_{CC}-V_L-V_{R1n}-V_{Ren}-V_o}{V_{CC}-2V_L-V_{R1n}-V_{Ren}-V_o}\ (V_L G_L+I_o) \qquad (2.19)$$

and

$$R_C = \frac{V_{CC}-2V_L-V_{R1n}-V_{Ren}-V_o}{(V_L G_L+I_o)} \quad . \qquad (2.20)$$

In (2.19) and (2.20), the values of the DC feedback voltage V_{R1n}, the AC feedback voltage V_{Ren}, and the saturation V_o and cut-off I_o offsets may be judiciously selected to satisfy the overall design constraints of a particular application.

The AC output voltage swing is given by

$$K_y V_L = \frac{I_{Cy}-I_o}{G_C+G_L} \quad \text{or} \quad I_{Cy} = K_y V_L (G_C+G_L) + I_o \text{ at } T_y \tag{2.21}$$

and $$K_x V_L = V_{CEx} - V_o - K_x V_{Ren} \quad \text{or}$$

$$V_{CEx} = K_x(V_L + V_{Ren}) + V_o \text{ at } T_x \tag{2.22}$$

Equations (2.09) and (2.21) give the DC operating point (I_{Cy}, V_{CEy}) at T_y, while (2.10) and (2.22) give the operating point (I_{Cx}, V_{CEx}) at T_x. The design of the input leg of the amplifier proceeds as described by (2.11) through (2.14).

Part 3 - Worst Case Tolerance Refinement

Considerable attention has been given to "worst case" design techniques which assure reliable circuit designs for specified component tolerance margins particularly for digital logic circuits[6]. While the effects of component tolerances are generally much more severe in linear circuits than in digital circuits, apparently, practical analytical techniques for worst case design of linear circuits are not in wide use at this time. It is felt that the demonstration of a straightforward worst case design theory for linear circuits may be of general value and is certainly of particular value in assuring that the already minimal dynamic range of a micropower amplifier is preserved in the face of component tolerances. In the case of broadband micropower amplifiers, the critical function of a worst case design technique is to insure that the worst possible combination of component tolerances will not result in I_{Cy} less than

$$\underline{I}_{Cy} = K_y V_L (1/\overline{R}_C + 1/R_L) + I_o \tag{2.23}$$

from (2.21) and V_{CEx} less than

$$\underline{V}_{CEx} = K_x (V_L + V_{Ren}) + V_o \tag{2.24}$$

from (2.22). (The symbolism $\underline{I}_{Cy}$ denotes the minimum value of the quantity I_{Cy} while $\overline{I}_{Cy}$ denotes its maximum value.)

Table II shows the worst case tolerances for the transistor, the biasing resistors and the supply voltage. From Table II and (2.09) it is evident that

$$V_{CEy} = \underline{V}_{CC} - \underline{I}_{Cy} (\overline{R}_1 + \overline{R}_C) \tag{2.25}$$

gives the value of V_{CEy} which accompanies $\underline{I}_{Cy}$ of (2.23). Also from (2.10)

$$I_{Cx} = \frac{\underline{V}_{CC} - \underline{V}_{CEx}}{\underline{R}_1 + \overline{R}_C} \tag{2.26}$$

gives the value of I_{Cx} which accompanies $\underline{V}_{CEx}$ of (2.24). From Table II and (2.11) and (2.12)

$$\underline{V}_{CC} = (\overline{I}_{By} + I_{2y}) \overline{R}_3 + I_{2y} \underline{R}_2 \tag{2.27}$$

$$0 = \overline{V}_{BEy} + I_{Ey} \overline{R}_1 - I_{2y} \underline{R}_2 \tag{2.28}$$

and T_y and

$$\underline{V}_{CC} = (\underline{I}_{Bx} + I_{2x}) \underline{R}_3 + I_{2x} \overline{R}_2 \tag{2.29}$$

$$0 = \underline{V}_{BEx} + I_{Ex} \underline{R}_1 - I_{2x} \overline{R}_2 \tag{2.30}$$

at T_x yield the values for R_2 and R_3 given in Appendix 1. In (2.27) through (2.30), $\overline{R}_1 = R_1 (1+\delta_R)$, $\underline{R}_1 = R_1 (1-\delta_R)$, $\underline{V}_{CC} = V_{CC} (1-\delta_V)$, and so forth where, for example, $\delta_R = 0.05$ for a $\pm 5\%$ resistor tolerance margin. Also, $\overline{I}_{By}$ indicates the largest transistor I_B at T_y considering both temperature effects and manufacturing and aging tolerances. The solutions to (2.27) through (2.30) give the nominal values of R_2 and R_3 which insure that I_{Cy} and V_{CEx} will not be less than the required values for the specified dynamic range, $K_y V_L$ at T_y and $K_x V_L$ at T_x, for the worst combination of tolerances which may arise. This design procedure may be applied to temperature, manufacturing and aging tolerances for all circuit elements including the transistor, the resistors, and the supply voltage.

Part 4 - Amplifier AC Characteristics

The purpose of Part 4 is to present an analysis of the small-signal AC characteristics of broadband amplifiers operating at microwatt power levels. A fourpole network approach as well as an equivalent circuit approach to the AC analysis will be outlined.

From Figure 11, using the familiar low-frequency fourpole "h" parameters to describe the transistor gives

$$v_1 = H_{11} i_1 + H_{12} v_2$$

and $$i_2 = H_{21} i_1 + H_{22} v_2 \tag{2.31}$$

where the approximate overall amplifier "H" parameters are given by Table III. (The exact values are listed in reference 7.) The amplifier H parameters are immediately useful in defining the gain and terminal impedances which are specified in Table IV. The H parameter characterization of the amplifier is valid, of course, only in the midband region.

In order to calculate the frequency response of a broadband micropower amplifier, it is convenient to utilize the hybrid pi transistor equivalent circuit previously developed in Section 1. Figure 12 shows the AC equivalent circuit of a single stage micropower broadband amplifier for its medium and high frequency ranges with $R_e = 0$. In view of the device impedance levels discussed in Section 1, $r_{b'}$ will be assumed negligible. Following this assumption, the principal question to be answered is whether or not the "Miller effect" approximation[8] may be used to unilateralize the amplifier*.

To determine this, an exact analysis of the circuit of Figure 12 under the noncritical assumptions that R_g, $R_{23} >> r_{b'e}$ and $R_C >> R_L$ yields

$$A_i = \frac{i_2}{i_1} = h_{fe} \frac{(1-j\omega \frac{r_{b'e}}{h_{fe}} C_C)}{1+j\omega r_{b'e}\left\{C_{b'e}+(1+h_{fe}\frac{R_L}{r_{b'e}}+j\omega R_L C_{b'e})C_C\right\}} . \quad (2.32)$$

A comparison of the breakpoints of this expression shows that for typical micropower amplifiers an accurate approximation over the useful frequency band of the amplifier is

$$\frac{i_2}{i_1} = h_{fe} \frac{1}{1+j\omega r_{b'e}\left\{C_{b'e}+(1+h_{fe}\frac{R_L}{r_{b'e}})\,C_C\right\}} . \quad (2.33)$$

Again under the noncritical assumptions R_g, $R_{23} >> r_{b'e}$ and $R_C >> R_L$, an exact analysis of the circuit of Figure 13 which employs the full Miller effect approximation also yields the result expressed by (2.33). Therefore, it appears that the usual Miller effect approximation for unilateralizing broadband amplifiers remains valid for microwatt power levels.

*The principal value of the Miller effect approximation is that it permits unilateralization of the amplifier with its accompanying simplification of the analysis. Referring to Figure 12, to retain accuracy in making this approximation it is necessary that: 1) C_C does not load the output generator $g_m V_{b'e}$ (i.e., $\frac{1}{j\omega C_C} >> \frac{R_C R_L}{R_C+R_L}$), and 2) the direct transmission through C_C be small compared to $g_m V_{b'e}$. An additional requirement for accuracy if the equivalent input capacitance of C_C [i.e., $C_C(1+g_m \frac{R_C R_L}{R_C+R_L})$] is shunted directly to ground is that $\frac{R_C R_L}{R_C+R_L}(1+g_m\frac{R_C R_L}{R_C+R_L})^{-1} \angle \left| j\omega C_C(1+g_m \frac{R_C R_L}{R_C+R_L}) \right|$.

By dropping the simplifying assumptions for R_g, R_{23}, and R_C, one finds from Figure 13 neglecting C_{ces}

$$\frac{i_2}{i_1} = \frac{h_{fe}/1+R_L/R_C}{1+r_{b'e}/R_{23}+j\omega\, r_{b'e}\left[(C_{b'e}+C_{b'es})+(1+\frac{h_{fe}}{r_{b'e}}\,\frac{R_CR_L}{R_C+R_L})(C_C+C_{Cs})\right]} \tag{2.34}$$

$$\text{with } \omega_{3db} = \frac{1+r_{b'e}/R_{23}}{r_{b'e}\left[(C_{b'e}+C_{b'es})+(1+\frac{h_{fe}}{r_{b'e}}\,\frac{R_CR_L}{R_C+R_L})(C_C+C_{Cs})\right]} \tag{2.35}$$

For the voltage gain

$$A_v = \frac{v_2}{v_1} = -\frac{h_{fe}\,(R_L/r_{b'e})}{1+R_L/R_C+j\omega R_L C_{ces}} \tag{2.36}$$

where $C_{b'es}$, C_{Cs}, and C_{ces} are the stray circuit capacitances in parallel with $C_{b'e}$, C_C and R_L respectively. (The stray capacitances are not shown on Figures 12 and 13.) From these equations, the product of the midband power gain and the effective bandwidth is, in absolute value,

$$\left(\frac{i_2}{i_1}\right)_{M.B.}\left(\frac{v_2}{v_1}\right)_{M.B.}\omega_{3db} = \frac{(\frac{h_{fe}}{1+R_L/R_C})^2\,R_L/r_{b'e}}{r_{b'e}\left[(C_{b'e}+C_{b'es})+(1+\frac{h_{fe}}{r_{b'e}}\,\frac{R_CR_L}{R_C+R_L})(C_C+C_{Cs})\right]} \tag{2.37}$$

Assuming

$$\frac{h_{fe}}{r_{b'e}}\,\frac{R_CR_L}{R_C+R_L} \simeq \frac{1}{r_f}\,\frac{R_CR_L}{R_C+R_L} >> 1 \text{ and } C_{b'e}+C_{b'es} \simeq C_C+C_{Cs},$$

$$\left(\frac{i_2}{i_1}\right)_{M.B.}\left(\frac{v_2}{v_1}\right)_{M.B.}\omega_{3db} \simeq \frac{1}{r_f\,(C_C+C_{Cs})}\,\frac{1}{1+R_L/R_C} \tag{2.38}$$

or $$G\omega_{3db} \simeq \frac{q}{kT}\,\frac{I_C}{(C_C+C_{Cs})}\,\frac{1}{1+R_L/R_C}$$

An examination of (2.38) indicates the gain-bandwidth product of a common emitter micropower amplifier can be improved by increasing the transistor collector current I_C, which increases power dissipation, and decreasing the transistor collector-to-base barrier capacitance C_C as well as the collector-to-base circuit stray capacitance C_{Cs}. Since C_C is usually of the order of 5 picofarads or less, the importance of minimizing the stray circuit capacitance

C_{Cs} in order to maximize gain-bandwidth product is quite clear. The frequency response of the circuit of Figure 8 when $R_e \neq 0$ is indicated in Appendix 2.

As an additional point of interest, the low frequency cut-off ω_{LF} of a micropower amplifier which should be caused by C_E will be calculated. From Figures 8 and 13

$$\frac{i_b}{i_g} = \frac{R_s}{R_s+r_{b'e}} \quad \frac{1+j\omega R_E C_E}{\left[\frac{R_s+r_{b'e}+(h_{fe}+1)R_E}{R_s+r_{b'e}}\right] + j\omega R_E C_E} \tag{2.39}$$

where $R_s = \dfrac{R_g R_{23}}{R_g+R_{23}}$ gives

$$\omega_{LF} = \frac{1}{R_E C_E} \quad \frac{R_s+r_{b'e}+(h_{fe}+1)R_E}{R_s+r_{b'e}} \; . \tag{2.40}$$

A final parameter which is useful in comparing the performance of micropower amplifiers is given by

$$F.M. = \frac{G\omega_{3db}}{P_D} \tag{2.41}$$

where $P_D = V_{CC}\left[I_E+I_2\right] = V_{CC}\left[I_E + \dfrac{V_{BE}+I_E R_1}{R_2}\right]$. (2.42)

This quotient of gain-bandwidth product and power dissipation can be considered as a figure of merit, F.M., for micropower amplifiers. In virtually all instances, a major objective in the design of a broadband micropower amplifier is to achieve a maximum gain and a specified bandwidth for a minimum power dissipation. Therefore, (2.41) defines a parameter whose relative magnitude is a useful indication of the quality of a given micropower amplifier design.

Part 5 - AC Temperature Compensation

Previous parts of this section have been concerned with DC and large-signal AC stabilization of micropower transistor amplifiers. Specifically, the DC operating point and the AC power output capability of an amplifier have been stabilized against changes with temperature and manufacturing tolerances in the transistor DC parameters I_{CBO}, h_{FE} and g_{BE}, as well as the values of the resistors R_1, R_2, R_3 and R_C and the supply voltage V_{CC}. However, the large temperature variations which occur in the small-signal fourpole h parameters of the transistor can give rise to large changes in the small-signal terminal properties of a micropower amplifier. The purpose

of Part 5 is to briefly outline a design theory[4] which has been developed for temperature compensation of the current gain, voltage gain, power gain, input impedance and output impedance of micropower amplifiers.

In order to simplify the presentation of the AC temperature compensation technique, component manufacturing and aging tolerances will be neglected and only temperature effects will be considered. A convenient method for handling the temperature changes is illustrated in Figure 14. The temperature factors or γ factors are used to describe the overall temperature changes in the resistor values and supply voltage (e.g., $\gamma_1 \equiv \frac{R_1 \text{ at } T_x}{R_1 \text{ at } T_y}$). Since the amplifier H parameters determine its terminal properties, compensation may be sought by imposing the requirements that

$$H_{11y}=H_{11x},\ H_{21y}=H_{21x} \text{ and } H_{22y}=H_{22x} \quad . \tag{2.43}$$

H_{12} is neglected since its effect on circuit behavior at the low frequencies considered here is negligible. Substituting the H parameter values listed in Table III gives

$$\frac{(h_{11ey}+h_{21ey}R_e)\,R_{23}}{(h_{11ey}+h_{21ey}R_e)+R_{23}} = \frac{(h_{11ex}+h_{21ex}\gamma_e R_e)\,\gamma_{23}R_{23}}{(h_{11ex}+h_{21ex}\gamma_e R_e)+\gamma_{23}R_{23}} \tag{2.44}$$

$$\frac{(h_{21ey})R_{23}}{(h_{11ey}+h_{21ey}R_e)+R_{23}} = \frac{(h_{21ex})\gamma_{23}R_{23}}{(h_{11ex}+h_{21ex}\gamma_e R_e)+\gamma_{23}R_{23}} \tag{2.45}$$

and $$1/R_C = 1/\gamma_C R_C \tag{2.46}$$

where it has been assumed that $\gamma_2 = \gamma_3 = \gamma_{23}$. A most useful solution to (2.44), (2.45) and (2.46) results from equating numerators and denominators. From this

$$\gamma_{23} = h_{21ey}/h_{21ex} \tag{2.47}$$

$$R_e = \frac{\gamma_{23}R_{23}-h_{11ey}}{h_{21ey}} \quad \text{requires } \gamma_{23}R_{23} > h_{11ey} \tag{2.48}$$

$$\gamma_e = \frac{R_{23}-h_{11ex}}{R_{23}-\frac{h_{21ex}}{h_{21ey}}h_{11ey}} \quad \text{requires } R_{23} > h_{11ex} \tag{2.49}$$

and $$\gamma_c = 1 \quad . \tag{2.50}$$

To simplify the circuit implementation, it is desirable to achieve $\gamma_e = 1$ in (2.49) which requires that $\frac{h_{11ex}}{h_{11ey}} = \frac{h_{21ex}}{h_{21ey}}$. Since $h_{11e} \simeq h_{21e}h_{11b} \simeq h_{21e}r_e \simeq$

$h_{21e} \frac{kT}{qI_C}$, for $\gamma_e = 1$, the relationship

$$\frac{I_{Cx}}{I_{Cy}} = \frac{T_x+273}{T_y+273} \tag{2.51}$$

must be satisfied. In effect, to achieve $\gamma_e = 1$, the h_{11e} and h_{21e} temperature variations must track each other. This can be conveniently achieved by controlling the DC collector current change with temperature so that $h_{11b} \simeq r_e \simeq \frac{kT}{qI_C}$ is constant. (As (2.49) indicates, under the special condition $\gamma_{23} R_{23} = h_{11y}$, implementation may be further simplified by $R_e = 0$.) If one then selects $\gamma_V = 1$ and $\gamma_E = 1$, all temperature factors for the circuit are specified with the result that only two temperature sensitive components, R_2 and R_3, are required for the desired compensation. ($\gamma = 1$ indicates temperature invariance.) Furthermore, it is evident that both R_2 and R_3 should exhibit the same temperature factor, γ_{23}.

From (2.51) of the preceding paragraph, it is evident that the AC compensation requirements influence the DC stability of the circuit. In this case the output power capability constraint imposed in Part 1 must be treated differently as indicated in Appendix 3.

Part 6-Cascode Amplifier

Among the broadband micropower amplifier design constraints listed in the introductory portion of this section is the requirement for a specified bandwidth ω_{3db}. Equation (2.35) of Part 4 indicates the value of ω_{3db} in terms of AC circuit parameters. In practice for common emitter cascodes the "Miller Effect" capacitance $(1+\frac{h_{fe}}{r_{b'e}} \frac{R_C R_L}{R_C+R_L})$ (C_C+C_{Cs}) largely determines the value of ω_{3db} via the multiplying effect of $\frac{h_{fe}}{r_{b'e}} \frac{R_C R_L}{R_C+R_L} >> 1$ on (C_C+C_{Cs}). Therefore, presuming the smallest practical value of (C_C+C_{Cs}), if a particular micropower amplifier design does not meet the specified ω_{3db}, an expedient approach to this objective is to reduce $\frac{R_C R_L}{R_C+R_L}$ by increasing the current and power drain of the amplifier. For example, in the common case where R_L represents the input impedance of the following stage, an increase in the collector current of the following stage reduces R_L and therefore R_C by the design procedure of Part 1. In this manner, one may trade power drain for bandwidth as well as gain-bandwidth product as indicated in (2.38).

A common-emitter, common-base cascode circuit which has been found to be particularly effective in reducing the Miller Effect capacitance to produce significantly larger bandwidths for essentially the same power gain and only a slight increase in power drain, compared with a single common

emitter stage, is shown in Figure 15. Referring to the schematic diagram of Part a of Figure 15, it is evident that T_1 and T_2 represent a direct coupled common-emitter, common-base cascode. C_1 and C_4 serve as bypass capacitors. The AC equivalent circuit of this cascode is shown in Part b of Figure 15. The stray collector-to-emitter capacitance of T_2, C_{ces2}, is neglected since it is not significant within the useful frequency range of the amplifier. An analysis of the AC equivalent circuit shows

$$\frac{i_2}{i_1} = \left(\frac{h_{fe1}}{1+r_{b'e1}/R_{23}+j\omega\, r_{b'e}C_p}\right)\left(\frac{h_{fb2}}{1+j\omega\, r_{\epsilon\,2}C_q}\right)\left(\frac{1}{1+R_L/R_C+j\omega\, R_L C_r}\right). \tag{2.52}$$

Ordinarily, $\dfrac{1+r_{b'e1}/R_{23}}{r_{b'e1}C_p} < < \dfrac{1+R_L/R_C}{R_L C_r} << \dfrac{1}{r_{\epsilon\,2}C_q}$

$$h_{fb2} \cong 1 \text{ and } g_{m1}r_{\epsilon\,2} \cong h_{fb1}\,\frac{r_{\epsilon\,2}}{r_{\epsilon\,1}} \cong 1$$

so that (2.52) gives

$$\frac{i_2}{i_1} = \frac{h_{fe1}/1+R_L/R_C}{1+r_{b'e1}/R_{23}+j\omega\, r_{b'e1}\left[(C_{b'e1}+C_{b'els})+2(C_{C1}+C_{Csl})\right]} \tag{2.53}$$

with $$\omega_{3db} = \frac{1+r_{b'e1}/R_{23}}{r_{b'e1}\left[(C_{b'e1}+C_{b'els})+2(C_{C1}+C_{Csl})\right]} \tag{2.54}$$

and $$\frac{v_2}{v_1} = -\frac{h_{fe1}(R_L/r_{b'e1})}{1+R_L/R_C+j\omega R_L(C_{C2}+C_{Cs2})}\,. \tag{2.55}$$

The similarity between the above equations and (2.34), (2.35) and (2.36) is immediately evident. The key result is that the Miller Effect multiplier has been reduced from $(1+\frac{h_{fe}}{r_{b'e}}\,\frac{R_C R_L}{R_C+R_L})$, which often exceeds 20, to a value of 2. This results in substantial increases in ω_{3db} while A_i and A_v are virtually unchanged.

The approximate value of the bypass capacitor C_4 may be calculated from Figure 15. Since

$$\frac{V_{be2}}{g_{m1}V_{be1}} = r_{\epsilon\,2}\,\frac{1+(1-h_{fb2})\,\frac{R_{45}}{r_{\epsilon\,2}}+j\omega R_{45}C_4}{1+j\omega R_{45}C_4} \tag{2.56}$$

where $R_{45} = \dfrac{R_4 R_5}{R_4+R_5}$,

$$C_4 = \frac{1}{\omega_{LF}} \quad \frac{1+(1-h_{fb2})\frac{R_{45}}{r_{e2}}}{R_{45}} \tag{2.57}$$

where ω_{LF} is given by (2.40).

The circuit of Figure 15 is of sufficient interest as a broadband micropower amplifier that the remaining features of its design will now be outlined. The DC equation for the output leg, analogous to (2.01) is

$$V_{CC} = I_{C2n}R_C + V_{CB2n} + (V_{BE2n} + V_{CE1n} + V_{R1n}) \tag{2.58}$$

where $V_{R1n} = I_{E1n}R_1 \cong I_{C1n}R_1 = I_{E2n}R_1 \cong I_{C2n}R_1$.

The AC LL, analogous to (2.02), of T_2 is

$$I_{C2n} = -(G_C + G_L)\, V_{CB2n} \quad . \tag{2.59}$$

Now, the locus of AC LL midpoints, analogous to (2.03), of T_2 is

$$I_{C2n} = (G_C + G_L)\, V_{CB2n} \quad . \tag{2.60}$$

Since $$V_{CB2n} = V_L = I_L/G_L \tag{2.61}$$

analogous to (2.04), substituting (2.61) into (2.58) and (2.60) gives

$$I_{Cn} = V_L G_L \frac{\left[V_{CC} - V_L - (V_{BE2n} + V_{CE1n} + V_{R1n})\right]}{\left[V_{CC} - 2V_L - (V_{BE2n} + V_{CE1n} + V_{R1n})\right]} \tag{2.62}$$

and $$R_C = \frac{\left[V_{CC} - 2V_L - (V_{BE2n} + V_{CE1n} + V_{R1n})\right]}{V_L G_L} \tag{2.63}$$

which are analogous to (2.05) and (2.06). In order to evaluate (2.62) and (2.63), the quantity $(V_{BE2n} + V_{CE1n} + V_{R1n})$ must be assigned a value. Since I_L is known, by assuming a minimum nominal operating temperature T_n, a conservative value for V_{BE2n} may be estimated. From Figure 15 it is evident that $v_{ce1n} = v_{be2n}$. The collector-to-emitter AC voltage swing of T_1 (v_{ce1n}) is quite small so that V_{CE1} may be selected at some constant nominal value such as 1.0 v which assures that T_1 remains out of the saturation region at all temperatures. As in Part 1, a practical procedure for selecting V_{R1n} is to compute and compare complete designs for several values.

With I_{Cn} and R_C calculated, the amplifier design proceeds in a manner directly analogous to the approach of Part 1. Considering the saturation, cut-off, and feedback refinements of Part 2, the design of the cascode amplifier again proceeds in a directly analogous manner with the advantage that the saturation V_o and cut-off I_o offset values may be reduced for the

common base connection. Tolerances may be treated in a fashion similar to the procedure of Part 3 and temperature compensation follows the pattern of Part 5. On the basis of simplicity, flexibility and performance, it appears that the cascode circuit of Figure 15 may be considered as a general replacement of the common emitter amplifier of Figure 8 in micropower applications.

SECTION 3 - AMPLIFIER PERFORMANCE

In this section typical experimental and calculated results based on the characterization data of Section 1 and the design theory of Section 2 are presented. Table V shows the detailed design and performance of five selected micropower amplifiers which illustrate the major features of Section 2. The assumed initial constraints are indicative of what might be expected from a high performance micropower amplifier. The data indicate that useful operating characteristics can be achieved at micropower levels and that the agreement between calculated and measured performance appears to support the design theory of Section 2.

Figure 16 illustrates the temperature behavior of the DC operating point of the circuits of columns 1 and 2 of Table V. As indicated in Table V, the agreement between predicted and measured performance at the operating temperature limits appears acceptable, while Figure 16 shows that intermediate performance is also well behaved.

The temperature variation of the total percent amplitude distortion % D in the output waveform of the amplifiers of columns 1 and 2 of Table V is illustrated in Figure 17. The measured peak output voltage V_2 was maintained at a constant value for all temperatures. The total distortion is rather large for two reasons. First, the variation of the forward current transfer ratio h_{fe} with I_C is quite pronounced at microampere current levels as illustrated by Figures 1 and 4. Near the maximum in the h_{fe} versus I_C curve, which occurs typically in the milliampere range, h_{fe} varies much more slowly. The second reason for the large distortion is the fact that the source internal impedance, R_g=50KΩ, used in gathering the data for Figure 17 is not the optimum value for minimizing the combined input and transfer distortion of the transistor. Due to the monotonic increase in h_{fe} and decrease in h_{ie} with increasing I_C at microampere current levels, current source signal, which completely eliminates input distortion, results in the smallest total % D. For example, by increasing R_g from 50KΩ to 500KΩ, the room temperature distortion in the first amplifier (R_e=0) with V_L=0.18v is reduced from 16% to 13%. Figure 17 shows that a 50% reduction in the actual peak output voltage from 0.6 V_L=0.18v to 0.3 V_L=0.09v causes a nearly equal percentage reduction in distortion. This response supports the anticipated result for the design procedure that primarily input and transfer characteristic nonlinearities in the active region rather than more sharply defined saturation and cut-off limits cause the distortion. The increased distortion at low temperatures and small collector currents is due to the more rapid rate of change of h_{fe} with I_C which occurs under these conditions. The usual reduction in distortion provided by degenerative feedback is readily apparent in Figure 17 for the curves of the second circuit where R_e=3.89KΩ.

Figures 18 and 19 indicate the variations of mid-band power gain G and input impedance R_i with temperature for the amplifiers of columns 1,

2 and 4 of Table V. The pronounced temperature sensitivity of the AC terminal characteristics of the two noncompensated ($\gamma_{23}=1.0$) micropower amplifiers is evident. For the amplifier without feedback, G increases by 4.7 db from 23.3 db to 28.0 db and R_i increases 274% from 106KΩ to 290KΩ for $-50 < T < 100^{\circ}C$. In the feedback case, temperature variations are somewhat reduced since G increases with temperature by 3.4 db from 19.6 db to 23.0 db and R_i increases 257% from 192KΩ to 494KΩ from $-50 \leq T \leq 100^{\circ}C$. The variation of power gain with temperature is due primarily to changes in current gain A_i, which are in turn due to h_{21e}, since voltage gain A_v as defined in Table IV remains relatively constant for both $R_e=0$ and 3.89KΩ. The variation of R_i is caused mainly by the variations of h_{11e} and $h_{21e}R_e$ which are in turn also due to h_{21e} since $h_{11e} \simeq h_{21e}h_{11b}$.

Figures 18 and 19 also show that the temperature compensated amplifier of column 4 of Table V, with $R_e=4.42K\Omega$ and $\gamma_{23}=0.28$, can provide quite useful values of G and R_i which are virtually unchanged for $-50 \leq T \leq 100^{\circ}C$. This pronounced temperature insensitivity can be achieved by the simple expedient of using a resistor-thermistor combination for R_2 and R_3. In addition, it is highly predictable as the data of Table V indicate.

The influence of the DC external emitter feedback voltage V_{R1n} at the nominal temperature T_n and the dynamic range constant $K_x = K_y = K$ on the performance of a micropower amplifier is illustrated by Figures 20 and 21. Figure 20 indicates that for a given K there is an optimum range of values of V_{R1n} for which upper temperature power gain G_x is essentially a maximum and upper temperature power drain P_{Dx} is essentially a minimum. For K=0.7, this value of V_{R1n} is approximately 1.40v. For small V_{R1n}, the fall-off of G_x and the increase in P_{Dx} are due to the small values for R_2 and R_3 which accompany small V_{R1n}. For large V_{R1n}, increasing I_C and decreasing R_C degrade the performance. As K decreases, the curves show the desirable results that G_x increases and P_{Dx} decreases. However, smaller values of K imply a smaller dynamic range for the amplifier at its temperature limits, T_y and T_x, as well as a larger operating point drift. It is apparent from the G_x and P_{Dx} curves that high performance circuit designs are more easily obtained at lower K values where the value of V_{R1n} is not so critical.

Figure 21 illustrates the dependence on V_{R1n} of upper temperature input impedance R_{ix} and output impedance R_{ox}. For a constant K, small V_{R1n} cause low values of R_2 and R_3 and therefore low values of R_{ix}. The fall-off of R_{ix} at large V_{R1n} is due to the small values of R_3 necessary to maintain the required base voltage as well as a smaller h_{11ex} due to larger I_{Cx} values. R_{ox} decreases monotonically with V_{R1n} due to decreases in R_C. The increase of R_{ix} with decreasing K is due to the greater operating point drift which accompanies smaller K and permits larger R_2 and R_3. The decrease of R_{ox} with increasing K is due to the smaller R_C values caused by the increases in V_{R1n} required to maintain the tight DC stabilities associated with larger K values.

The effect of resistor manufacturing tolerances on the design and performance of a typical linear broadband micropower amplifier is indicated in column 3 of Table V. The measured results were achieved using two 10% worst case design circuits whose resistor values were deliberately chosen to be at their worst values at T_y= -50°C and at T_x= +100°C as noted in Table II. The agreement between calculated and measured performance indicated in Table V appears to substantiate the worst case design theory of Part 3 of Section 2.

In Table VI the calculated effects of tolerances in the values of R_1, R_2, R_3 and R_C on the design of a micropower amplifier are indicated in detail. The minimum power 0% tolerance (δ_R=0, δ_{CR}=0) design with K=0.5 corresponds to the circuit of the first column of Table V while the δ_R=0.10, δ_{CR}=0 design corresponds to the circuit of the third column. It is quite evident from Table VI that the relatively loose DC operating point stability associated with K=0.5 permits large values of R_2 and R_3 when δ_R=0. Consequently, the reductions in R_2 and R_3 necessary to combat worst case tolerances up to 10% and above are readily possible with little increase in total power dissipation. This fact is also illustrated by the δ_R=0.02, K=0.5 and δ_R=0.02, K=0.7 curves of Figure 22. Therefore, the worst case K=.5 calculated results of Table VI and Figure 22 indicate that by permitting a sufficiently loose DC stability micropower amplifiers can readily be designed to accept 10% worst case resistor tolerances and maintain a reasonable (one half full range) dynamic range for a 150°C temperature change. As indicated by the lower portion of Table VI containing the minimum power designs and Figure 22, by adjusting the value of V_{R1n} it is possible to minimize the power drain of a circuit designed with a given resistor tolerance margin. (It should be noted that the worst case conditions assumed in Part 3 of Section 2 which form the basis for column 3 of Table V as well as Figure 22 and Table VI, are indeed more severe than any physically realizable set of tolerances. The reason for this, obviously, is that any given circuit can have either one but not both the worst set of tolerances for $\underline{I}_{Cy}$ and $\underline{V}_{CEx}$, as indicated in Table II. Consequently, the design theory for resistor tolerances is highly conservative.)

In microelectronic integrated circuits where the resistors are fabricated by batch processes such as evaporation of thin films of metals or diffusion of impurities into silicon substrates, it is frequently the case that the absolute resistor values exhibit wide tolerances but the relative values or ratios of the resistors to each other are virtually constant. Such constant ratio tolerances are not as severe as true worst case tolerances, and a comparison of the minimum power worst case and constant ratio designs of Table VI shows this fact. A linear micropower amplifier can withstand worst case tolerances of 2% or δ_R=0.02 combined with constant ratio tolerances of 20% or δ_{CR}=0.20 and larger as indicated by Table VI and Figure 22. With regard to the physical realizability of the constant ratio tolerances assumed in the calculation for Table VI, the remarks of the previous paragraph again apply.

Columns 1 and 5 of Table V and Figures 23 through 26 provide a comparison of the vital features of the basic common emitter amplifier and the cascode amplifier with improved frequency response. Figure 23 shows that, for typical circuits of equal maximum output power capability, the power drain of a cascode amplifier is less than twice the drain of a common emitter amplifier. Figure 24 shows that the power gain of a cascode amplifier suffers only a slight reduction of about 0.5 db compared with the common emitter amplifier. Figure 25 illustrates the key advantage of the cascode stage which is a five-to-ten time increase in cut-off frequency compared with a common emitter stage. An overall measure of the comparative performance of the common emitter and cascode amplifiers is indicated in Figure 26. The gain-bandwidth product divided by power drain provides a Figure of Merit which indicates the overall superior performance of the cascode amplifier.

It is evident from Figures 23 through 26 that the principal advantage of the cascode amplifier is its comparatively large bandwidth. In practice, stray circuit capacitances which are neglected in Figures 23 through 26 severely degrade this bandwidth. For example, the stray capacitances present in the relatively crude experimental circuits on which Table V is based were larger than the transistor capacitances which are comparable to those of device D. In order to determine the device limited frequency potential of the circuits, stray circuit capacitance was neglected in the calculated performance and the measured performance data were corrected for the effects of stray circuit capacitance. To illustrate the significance of this correction, the directly measured or uncorrected bandwidths of the amplifiers of columns 1 and 5 of Table V were 15 KC and 50 KC respectively at room temperature. If these results are corrected to remove the influence of measured stray circuit capacitances, the corresponding bandwidths are about 25 KC and 120 KC, respectively, at room temperature. Consequently, it is apparent that the latest advances in microelectronic packaging techniques are necessary in order to properly exploit present micropower transistor capabilities and approach the predicted behavior of Figure 25.

CONCLUSIONS

This report provides a rather comprehensive discussion of the static and dynamic design and performance of micropower transistor broadband linear amplifiers. The initial consideration in an amplifier design is the characterization of a micropower transistor. The salient features of the micropower transistors described in Section 1 are:

1. Junction reverse currents less than one nanoampere at room temperature.

2. Forward current transfer ratios, h_{FE} and h_{fe}, greater than 50 for collector currents of 1 to 10μa.

3. Increased sensitivity of the DC forward current transfer ratio h_{FE} and the fourpole parameters h_{11e} and h_{21e} to quiescent collector current and temperature changes.

4. A relatively limited gain-bandwidth product f_T.

5. A simple hybrid pi common emitter small-signal equivalent circuit essentially consisting of the junction barrier capacitances, C_{Te} and C_C, the diffusion resistance, $r_{b'e}$, and the output current generator $g_m V_{b'e}$.

Assuming that constraints exist on the supply voltage, load impedance, output voltage swing, operating temperature range, DC power drain and bandwidth of a micropower amplifier, suitable designs can be generated by means of the procedure outlined in Section 2. With regard to DC design, operating point stabilization is affected by: 1) I_{CBO} which may be comparable to I_B, if not I_C, at temperatures of 100°C and above; 2) increased temperature sensitivity of h_{FE}; and 3) large temperature induced changes in V_{BE}. Large-signal AC design is critical due to the restricted dynamic range imposed by microampere collector currents and low collector voltages. In this connection, DC operating point drift, saturation and cut-off effects in the transistor and both transistor and resistor tolerances must be considered. Small-signal AC performance is adversely affected by the limited gain-bandwidth product of micropower transistors as well as the increased temperature sensitivity of their small-signal fourpole parameters.

A key element in the micropower amplifier design procedure of Section 2 is the simple but rather rigorous approach used to unify the DC and large-signal AC design of an amplifier. Subject to initial constraints, the procedure yields an optimum circuit design in that it: 1) provides a specified output power capability over the design temperature range, 2) minimizes amplifier power drain, and 3) maximizes amplifier power gain. An additional feature of the design procedure is its adaptability to a worst case treatment of the effects of saturation and cut-off in the transistor and manufacturing and aging tolerances in all circuit elements.

In the small-signal analysis and design of broadband micropower amplifiers, a unilateralized hybrid pi transistor equivalent circuit can be utilized. Pronounced temperature variations in amplifier low-frequency AC terminal characteristics may be accurately compensated by means of a combination of emitter degenerative feedback and temperature sensitive base voltage-divider resistors. The bandwidth of common emitter micropower amplifiers is limited by the Miller Effect capacitance and may be enhanced by increased transistor quiescent current and by employing common emitter - common base cascode circuits to reduce the Miller capacitance multiplier. This later technique may be widely used to extend the bandwidth of micropower circuits without sacrificing gain or additional power drain.

On the basis of the results described in this report, it is evident that the principal obstacle to be overcome in the application of micropower transistors in portable military communications equipment is the limited gain-bandwidth product of micropower devices and circuits. In order to improve device and circuit frequency response, transistor junction capacitances, header capacitances and stray circuit capacitances must be reduced by at least an order of magnitude to about 0.1 pf. The accomplishment of this objective does appear feasible if the latest advances in microelectronic device fabrication and packaging are brought to bear on the problem. Further reductions in transistor active region lateral dimensions, perfection of surface passivation techniques in order to obviate current package forms and development of passive parts and interconnections with dimensions comparable to the transistor are the principal necessary steps toward practical micropower communications circuits and equipments.

ACKNOWLEDGMENTS

The authors gratefully acknowledge the many invaluable contributions of Mr. William J. Fox to the final outcome of the work described in this report. In addition, the assistance of Mr. Robert Farlee with the transistor characterization and Mr. James Oeffinger with the calculation of circuit designs is acknowledged.

REFERENCES

1. "Electrons and Holes in Semiconductors," W. Schockley; D. Van Nostrand, Princeton, New Jersey, pp 309 - 318, 1950.

2. "Low Current Alpha in Silicon Transistors," J. E. Iwerson et al; IRE Transactions on Electron Devices, Vol. ED-9, No. 6, pp 474 - 478, November 1962.

3. "Transistor Electronics," DeWitt and Rossoff; McGraw-Hill, New York, pp 112 - 115, 328 - 332, 1957.

4. "Transistor Electronics," A. W. Lo et al; Prentice Hall, Englewood, New Jersey, pp 169 - 178, 1955.

5. "Optimum Stabilization Networks for Functional Electronic Blocks," J. D. Meindl and O. Pitzalis; Proceedings of NEC, Vol. 16, Chicago, Illinois, pp 576 - 590, October 1960.

6. "Design of Transistorized Circuits for Digital Computers," A. I. Pressman; J. F. Rider, Inc., New York, pp 93 - 249, 1959.

7. "Power Dissipation in Microelectronic Transmission Circuits," J. D. Meindl, IRE Transactions on Military Electronics, Vol. MIL-5, pp 209 - 215, July 1961.

8. "Transistor Circuit Analysis," Joyce and Clark; Addison Wesley, Inc., pp 248 - 257, 1961.

9. "AC Temperature Compensation of Integrated Amplifiers," J. D. Meindl and O. Pitzalis; IEEE Winter General Meeting, CP63-62, New York, January 1963.

"AC Temperature Compensation of Integrated Amplifiers," J. D. Meindl and O. Pitzalis; U. S. Army Electronics Research and Development Laboratory Technical Report 2307, Fort Monmouth, New Jersey, pp 1 - 6, September 1962.

APPENDIX 1

The general expressions for the base voltage divider resistors R_2 and R_3 considering the combined effects of manufacturing and aging tolerances and temperature variations in the transistor, resistors and supply voltage are

$$R_3 = \frac{V_{CC}(a_{11}R_1+d_1)+q\left[rR_1^2+b_3R_1+s\right]}{\alpha_3\beta_3\gamma_3(c_2R_1+b_2)} \tag{1a}$$

and

$$R_2 = \frac{\alpha_3 R_3(\alpha_1 R_1 I_{Ey}+V_{BEy})}{\alpha_2\left[\alpha_v V_{CC}-V_{BEy}-\alpha_1 R_1 I_{Ey}-\alpha_3 R_3 I_{By}\right]} \tag{2a}$$

where

$$a_{11} = \alpha_2\alpha_v\beta_1\beta_3\gamma_1\gamma_3 I_{Ex} - \alpha_1\alpha_3\beta_2\beta_v\gamma_2\gamma_v I_{Ey}$$

$$b_2 = \alpha_2 \bar{I}_{By} \underline{V}_{BEx} - \beta_2\gamma_2 \underline{I}_{Bx} \bar{V}_{BEy}$$

$$b_3 = \alpha_1 I_{Ey} \underline{V}_{BEx} + \beta_1\gamma_1 I_{Ex} \bar{V}_{BEy}$$

$$c_2 = \alpha_2\beta_1\gamma_1 \bar{I}_{By} I_{Ex} - \alpha_1\beta_2\gamma_2 \underline{I}_{Bx} I_{Ey}$$

$$d_1 = \alpha_2\alpha_v\beta_3\gamma_3 \underline{V}_{BEx} - \alpha_3\beta_2\beta_v\gamma_2\gamma_v \bar{V}_{BEy}$$

$$q = \alpha_3\beta_2\gamma_2 - \alpha_2\beta_3\gamma_3$$

$$r = \alpha_1\beta_1\gamma_1 I_{Ex} I_{Ey}$$

$$s = \underline{V}_{BEx} \bar{V}_{BEy}$$

and

$$\alpha_1 = (1+\delta_{R1}+\delta_{CR}) \qquad \beta_1 = (1-\delta_{R1}-\delta_{CR})$$

$$\alpha_2 = (1-\delta_{R2}+\delta_{CR}) \qquad \beta_2 = (1+\delta_{R2}-\delta_{CR})$$

$$\alpha_3 = (1+\delta_{R3}+\delta_{CR}) \qquad \beta_3 = (1-\delta_{R3}-\delta_{CR})$$

$$\alpha_v = (1-\delta_v) \qquad \beta_v = (1-\delta_v)$$

$$\gamma_1 = \frac{R_1 \text{ at } T_x}{R_1 \text{ at } T_y} \qquad \gamma_3 = \frac{R_3 \text{ at } T_x}{R_3 \text{ at } T_y}$$

$$\gamma_2 = \frac{R_2 \text{ at } T_x}{R_2 \text{ at } T_y} \qquad \gamma_v = \frac{V_{CC} \text{ at } T_x}{V_{CC} \text{ at } T_y}$$

In the preceding expressions:

a) δ_{R1}, δ_{R2} and δ_{R3} represent the worst case resistor manufacturing and aging tolerances.

b) δ_{CR} represents the constant ratio resistor manufacturing and aging tolerances.

c) δ_v represents the worst case supply voltage tolerance.

d) γ_1, γ_2 and γ_3 represent the resistor temperature factors.

e) γ_v represents the supply voltage temperature factor.

As examples of the evaluation of (1a) and (2a):

a) For $\pm$ 5% worst case resistor manufacturing and aging tolerances $\delta_{R1} = \delta_{R2} = \delta_{R3} = 0.05$, 0% constant ratio tolerance $\delta_{CR} = 0$, 0% supply voltage tolerance $\gamma_v = 0$ and no resistor or supply voltage temperature variation, $\gamma_1 = \gamma_2 = \gamma_3 = \gamma_v = 1.0$.

b) For $\pm$ 2% worst case resistor manufacturing and aging tolerances $\delta_{R1} = \delta_{R2} = \delta_{R3} = 0.02$, $\pm$ 10% constant ratio resistor manufacturing and aging tolerance $\delta_{CR} = 0.10$, $\pm$5% supply voltage tolerance $\delta_v = 0.05$, a 20% increase in all resistor values over the design temperature range $\gamma_1 = \gamma_2 = \gamma_3 = 1.20$ and a 5% decrease in the supply voltage over the design temperature range $\gamma_v = 0.95$.

In certain cases where temperature behavior is predictable, indicated in Part 5 of Section 2, it is advantageous to treat resistor manufacturing and aging tolerances separately from temperature variations via the temperature factors γ_1, γ_2, γ_3, γ_4 and γ_v. If the sign of a temperature variation is unknown, the magnitude must be included in δ in the worst case analysis.

APPENDIX 2

In the case where $R_e \neq 0$, the current and voltage gain of the circui
Figure 8 are given by (

$$\frac{i_2}{i_1} = \frac{g_{in} z_{b'e}}{1 + \frac{R_e + (1+g_m R_e) z_{b'e}}{R_{23}} + j\omega \left[R_e + (1+g_m R_e)\, z_{b'e} + g_m R_L z_{b'e} \right] (C_C + C_{}}$$

$$\text{and} \quad \frac{v_2}{v_1} = - \frac{g_m z_{b'e}}{R_e + z_{b'e}(1+g_m R_e)} \quad \frac{R_C Z_L}{R_C + Z_L} \tag{4a}$$

$$\text{where} \quad z_{b'e} = \frac{r_{b'e}}{1+j\omega\, r_{b'e}(C_{b'e}+C_{b'es})} \quad \text{and } Z_L = \frac{R_L}{1+j\omega R_L C_{ces}} \; .$$

APPENDIX 3

When the temperature compensation technique of Part 5 of Section 2 is utilized in an amplifier design, the AC output voltage swing, which is specified for the design, may be achieved as described below.

Assuming the temperature compensation constraints given by (2. 47) through (2. 51), the design proceeds as described by (2. 15) through (2. 20) of Part 2 of Section 2. If K_y is selected, I_{Cy} is determined by (2. 21). From this, (2. 51) gives I_{Cx} for the temperature compensated design. Therefore, (2. 10) yields V_{CEx} and (2. 22) then specifies the value of K_x which accompanies the compensated design. If this value of K_x does not provide a suitable output voltage swing, another value for V_{R1n} should be selected in (2. 19) and (2. 20) which will yield a new value for K_x. (An alternate approach is to select several values for $K_x = K_y$ until (2. 51) is satisfied.) R_2 and R_3 may then be computed from (1a) and (2a) of Appendix 1 where all α's, β's, and γ's are unity except $\gamma_2 = \gamma_3 = \gamma_{23}$. Finally, the R_e required for AC compensation may be computed from (2. 48).

It is important to note that in computing I_{Cn} and R_C from (2. 19) and (2. 20), a value was selected for V_{Ren} which, in effect, determined $R_e = R_{en}/(I_{Cn} - I_o)$. If this latter value of R_e is greater than the value required by (2. 48), the value given by (2. 48) should be used and the excess amount should be included in R_1 to be bypassed by C_1. In this way the AC dynamic range will be increased somewhat over the design value, and the desired AC compensation will be affected.

If the value of R_e computed from (2. 48) is greater than the value effectively assumed in (2. 19) and (2. 20), the recommended procedure is to return to (2. 19) and (2. 20) and increase the selected value of V_{Ren} and therefore R_e in order to precipitate the situation described in the previous paragraph.

TABLE I - MICROPOWER TRANSISTOR CHARACTERISTICS

	DC Characteristics						AC Characteristics																	
	I_C = 10 μa, V_{CE} = 3.0 v, I_B = 1.0 μa		I_C = 10 μa, V_{CE} = 3.0 v			V_{CB} = 3.0 v	I_C = 10 μa, V_{CE} = 3.0 v		I_C = 100 μa, V_{CE} = 3.0 v		I_C = 1.0 ma, V_{CE} = 3.0 v		I_C = 10 μa, V_{CE} = 3.0 v		I_C = 10 μa, V_{CE} = 3.0 v		I_C = 10 μa, V_{CE} = 3.0 v		I_C = 100 μa, V_{CE} = 3.0 v		I_C = 1.0 ma, V_{CE} = 3.0 v		C_{TE}, V_{BE} = +0.3 v, C_C, V_{CB} = -3.0 v, C_D, I_C = 1.0 ma		
T (°C) =	25		-50	25	100		25		25		25		-50		100		25		25		25		25		
Device	V_{CES} (V)	V_{BES} (V)	h_{FE}	h_{FE}	h_{FE}	I_{CBO} (na)	h_{11e} (KΩ)	h_{21e}	h_{11e} (KΩ)	h_{21e}	h_{11e} (KΩ)	h_{21e}	h_{11e} (KΩ)	h_{21e}	h_{11e} (KΩ)	h_{21e}	f_{3db} (KC)	f_T (MC)	f_{3db} (KC)	f_T (MC)	f_{3db} (KC)	f_T (MC)	C_{TE} pf	C_C pf	C_D pf
A	0.1	0.55	23.8	66.6	106	1.0	184	71.0	26	95.4	3.2	120	73	37	350	107.5	24	1.7	150	14.3	935	112	16.7	6.28	27.2
B	0.092	0.52	14.7	54.0	125	3.8	200	76	38	141	6.4	230	46	22.5	460	146	42	3.2	184	26	532	123	9.0	2.47	35.8
C	0.13	0.53	62.5	91.0	156	9.0	335	125	65	248	10.6	390	172	91.8	600	188	30	3.75	118	29.2	286	112	5.06	3.0	43.8
D	0.16	0.6	23.2	71.5	128	33.0	217	78	30	110	4.0	140	66	33.0	435	134	90	7.0	595	65.6	4290	600	2.13	1.32	5.67
E	0.05	0.49	20.0	50.0	96.5	14.0	187	68	37	130	5.8	210	61	30.0	400	121	44	3.0	200	26	675	142	8.87	2.82	29.1
F	0.13	0.52	58.9	115	192	30.0	330	124	43	159	4.6	172	138	71.6	545	173	16.1	2.0	90.5	14.3	470	81	16.4	4.6	51.0

Typical Characteristics		I_C = 10 μa, V_{CE} = 3.0 v			I_C = 1.0 ma, V_{CE} = 3.0 v
	T (°C) =	-50	25	100	25
	h_{12e} =	2.3×10^{-4}	5×10^{-4}	1×10^{-3}	3.2×10^{-4}
	h_{22e} (ohms)$^{-1}$ =	0.013×10^{-6}	0.02×10^{-6}	0.032×10^{-6}	16×10^{-6}

TABLE II - WORST CASE CONDITIONS *

		Transistor					Resistors and Supply Voltage				
		I_{CBo}	h_{FE}	g_{BE}	I_B	V_{BE}	R_1	R_2	R_3	R_C	V_{CC}
T_y	$\underline{I}_{CY}$	$\underline{I}_{CBo}$	$\underline{h}_{FE}$	$\underline{g}_{BE}$	$\bar{I}_B$	$\bar{V}_{BE}$	$\bar{R}_1$	$\underline{R}_2$	$\bar{R}_3$	$\bar{R}_C$	$\underline{V}_{CC}$
	$\bar{V}_{CEy}$	$\underline{I}_{CBo}$	$\underline{h}_{FE}$	$\underline{g}_{BE}$	$\bar{I}_B$	$\bar{V}_{BE}$	$\bar{R}_1$	$\underline{R}_2$	$\bar{R}_3$	$\underline{R}_C$	$\bar{V}_{CC}$
T_x	$\bar{I}_{Cx}$	$\bar{I}_{CBo}$	$\bar{h}_{FE}$	$\bar{g}_{BE}$	$\underline{I}_B$	$\underline{V}_{BE}$	$\underline{R}_1$	$\bar{R}_2$	$\underline{R}_3$	$\underline{R}_C$	$\bar{V}_{CC}$
	$\underline{V}_{CEx}$	$\bar{I}_{CBo}$	$\bar{h}_{FE}$	$\bar{g}_{BE}$	$\underline{I}_B$	$\underline{V}_{BE}$	$\underline{R}_1$	$\bar{R}_2$	$\underline{R}_3$	$\bar{R}_C$	$\underline{V}_{CC}$

* 1. The I_{CBo}, h_{FE} and g_{BE} values indicated are worst case from the viewpoint of causing a maximum operating point drift.

2. The I_B and V_{BE} values indicated are worst case from the viewpoint of maintaining a given operating point drift.

3. The R_1, R_2, R_3, R_C and V_{CC} values indicated are worst case from the viewpoint of maintaining a given operating point drift.

TABLE III - FOURPOLE H PARAMETERS

$H_{11} = \dfrac{\left[h_{11} + h_{21}R_e\right] R_{23}}{\Delta}$	$H_{12} = \dfrac{(h_{12} + h_{22}R_e) R_{23}}{\Delta}$
$H_{21} = \dfrac{h_{21}R_{23}}{\Delta}$	$H_{22} = 1/R_C$
$\Delta = (h_{11} + h_{21}R_e) + R_{23}$,	$\Delta^H = H_{11}H_{22}$

(Approximate values for $1/R_C > h_{22}$)

TABLE IV - AMPLIFIER AC CHARACTERISTICS

Current Gain	Voltage Gain	Power Gain
$A_i = \dfrac{i_2}{i_1} = \dfrac{H_{21}}{1 + H_{22}R_L} \simeq \dfrac{H_{21}}{1 + R_L/R_C}$	$A_v = \dfrac{v_2}{v_1} = \dfrac{-H_{21}R_L}{H_{11} + \Delta^H R_L} \simeq -\dfrac{H_{21}}{H_{11}} \dfrac{R_L}{(1 + R_L/R_C)}$	$G = \left(\dfrac{i_2}{i_1}\right)\left(\dfrac{v_2}{v_1}\right)$

Input Impedance	Output Impedance
$R_i = \dfrac{H_{11} + \Delta^H R_L}{1 + H_{22}R_L} \simeq H_{11}$	$R_o = \dfrac{H_{11} + R_g}{\Delta H + H_{22}R_g} \simeq \dfrac{1}{H_{22}} \simeq R_C$

TABLE V - AMPLIFIER PERFORMANCE DATA

		1. Basic Design with Offset		2. Feedback Design		3. Worst Case Design		4. Temperature Compensated Design		5. Cascode Design	
Circuit Constraints											
V_{CC}	(v)	3.0		3.0		3.0		3.0		4.0	
R_L, $R_{L'}$	(KΩ	50,50		50,50		50,50		50,50		50,50	
V_L	(v)	0.3		0.3		0.3		0.3		0.3	
T_y, T_x	(°C)	-50, +100		-50, +100		-50, +100		-50, +100		-50, + 100	
Circuit Design											
V_{Rln}	(v)	1.0		1.0		1.6		1.0		0.6	
V_{Rcn}	(v)	0.00		0.03		0.00		0.06**		0.00	
V_o	(v)	0.3		0.3		0.3		0.3		0.00	
I_o	(μa)	0.3		0.3		0.3		0.3		0.3	
I_{Cn}	(μa	8.02		8.02		10.1		8.12		7.75	
R_C	(KΩ	175		175		79.4		165		206	
$K = K_y = K_x$		0.6		0.6		0.5		0.6		0.5	
δ_R, δ_V		0,0		0,0		0.10,0		0,0		0,0	
R_1	(KΩ)	125		125		159		123		77.4	
R_e	(KΩ	0.0		3.89		0.0		4.42		0.0	
R_2, R_4	(MΩ	2.77,	-	2.56,	-	5.66,	-	1.74,	-	.343,	1.63
R_3, R_5	(MΩ	2.54,	-	2.45,	-	2.60,	-	1.79,	-	.930,	1.44
γ_{23}		1		1		1		.283		1	
Circuit Performance		C	M	C	M	C	M	C	M	C	M
I_{Cy}	(μa)	4.93	4.90	4.93	4.90	5.02	5.04	4.99	4.98	4.03	4.1
V_{CEy}	(v)	1.52	1.50	1.54	1.60	1.69	1.67	1.56	1.57	1.85	1.9
I_{Cx}	(μa)	8.42	8.40	8.46	8.48	11.1	11.0	8.62	8.61	8.63	8.6
V_{CEx}	(v)	0.48	0.50	0.45	0.44	0.45	0.47	0.516	0.52	0.55	0.6
P_{Dx}	(μw)	27.1	27.0	27.3	27.9	34.7	34.5	35.1	35.0	52.9	52.8
A_{iy}		21.3	21.5	19.6	18.9	17.3	16.0	17.9	17.7	14.4	12.3
A_{ix}		63.2	60.0	50.0	49.2	56.8	54.0	17.9	17.8	33.2	30.7
A_{vy}		9.98	10.0	5.0	4.96	8.02	8.0	4.62	4.58	8.68	7.15
A_{vx}		10.2	10.3	5.06	5.00	10.6	10.0	4.62	4.55	10.9	10.3
G_y	(db)	23.3	23.0	19.9	19.7	21.4	21.0	19.2	19.1	21.0	19.4
G_x	(db)	28.1	27.9	25.0	24.0	27.8	27.3	19.2	19.1	25.6	25.0
R_{iy}	(KΩ)	107	100	196	182	100	109	194	193	83.0	85.0
R_{ix}	(KΩ)	311	290	493	482	269	249	194	196	152	149
R_{oy}	(KΩ	175	-	175	-	86	-	165	-	206	-
R_{ox}	(KΩ	175	-	175	-	86	-	165	-	206	-
f_{3dby}*	(KC.)	48.3	39.	52.4	42.6	65	52.4	60 KC	48.4	218	162
f_{3dbx}*	(KC.)	10.1	9.9	12.5	12.2	17.4	17.0	41.7	40.8	110	82

* = Measured values corrected for stray circuit capacitance
** = Allowable value
C - calculated, M - measured

TABLE VI WORST CASE DESIGNS

δ_{CR}	δ_R	V_{Rln} (v)	R_1 (KΩ)	R_2 (MΩ)	R_3 (MΩ)	R_C (KΩ)	I_{Cy} (μa)	V_{CEy} (v)	I_{Cx} (μa)	V_{CEx} (v)	P_{Dx}
					Constant V_{Rln} Designs						
0.00	0.00	1.6	159	195.	8.00	79.4	5.19	1.76	10.7	.30	32.457
0.00	0.02	1.6	159	80.7	7.35	79.4	5.15	1.75	10.8	.30	32.7
0.00	0.05	1.6	159	32.2	6.08	79.4	5.10	1.73	10.9	.30	33.2
0.00	0.10	1.6	159	5.66	2.60	79.4	5.02	1.69	11.1	.30	34.7
0.05	0.00	1.6	159	102.	7.32	79.4	5.10	1.73	11.3	.30	34.2
0.10	0.00	1.6	159	67.4	6.70	79.4	5.02	1.69	11.9	.30	36.1
0.20	0.00	1.6	159	37.7	5.59	79.4	4.87	1.61	13.4	.30	40.7
0.10	0.02	1.6	159	38.4	6.00	79.4	4.99	1.67	12.0	.30	36.5
0.20	0.02	1.6	159	22.7	4.84	79.4	4.85	1.59	13.5	.30	41.2
					Minimum Power Designs						
0.00	0.00	0.8	103	3.99	4.45	206	4.03	1.75	8.24	.30	25.9
0.00	0.02	1.0	125	4.91	4.31	175	4.14	1.74	8.49	.30	26.6
0.00	0.05	1.2	143	3.80	2.95	143	4.30	1.71	8.93	.30	28.4
0.00	0.10	1.6	159	5.66	2.60	79.4	5.02	1.69	11.1	.30	34.7
0.05	0.00	0.9	114	5.14	4.75	190	4.05	1.70	8.81	.30	27.5
0.10	0.00	0.9	114	4.11	3.97	190	4.02	1.65	9.30	.30	29.2
0.20	0.00	0.9	114	2.57	2.66	190	3.96	1.55	10.5	.30	33.5
0.10	0.02	1.0	125	2.71	2.63	175	4.07	1.64	9.43	.30	30.3
0.20	0.02	1.1	134	2.54	2.18	159	4.07	1.54	10.9	.30	35.1

For all above designs $K = 0.5$, $V_{CC} = 3.0v$, $R_i = 50\ K\Omega$, $V_L = 0.3v$

$T_y = -50°C$, $T_x = 100°C$, $V_o = 0.3v$, $I_o = 0.3\mu a.$,

$V_{Ren} = 0.0v$, $\delta_V = 0.00$

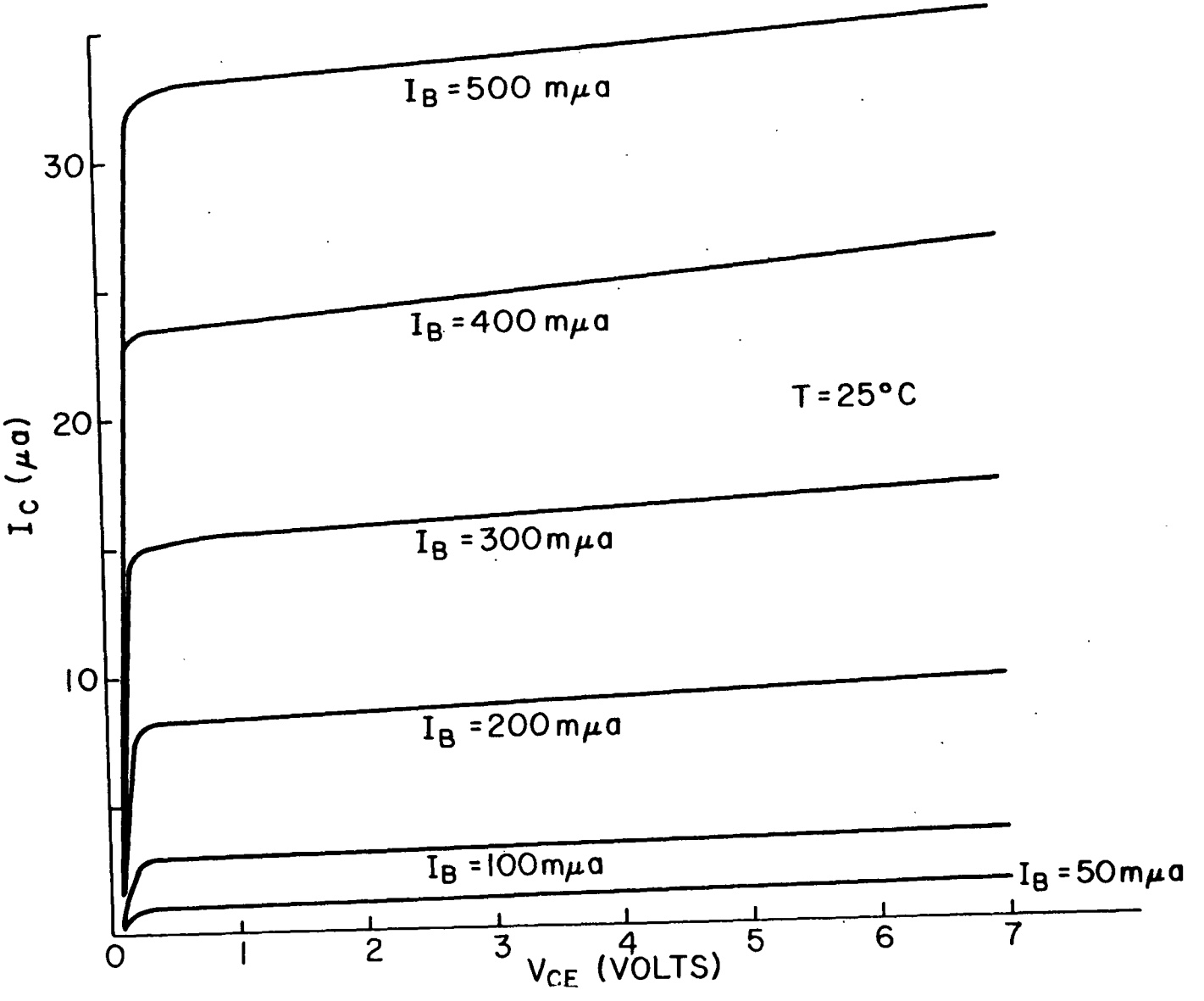


Figure 1 - Collector Characteristics for Common Emitter Configuration; collector current I_C versus collector-to-emitter voltage V_{CE} for various base currents I_B.

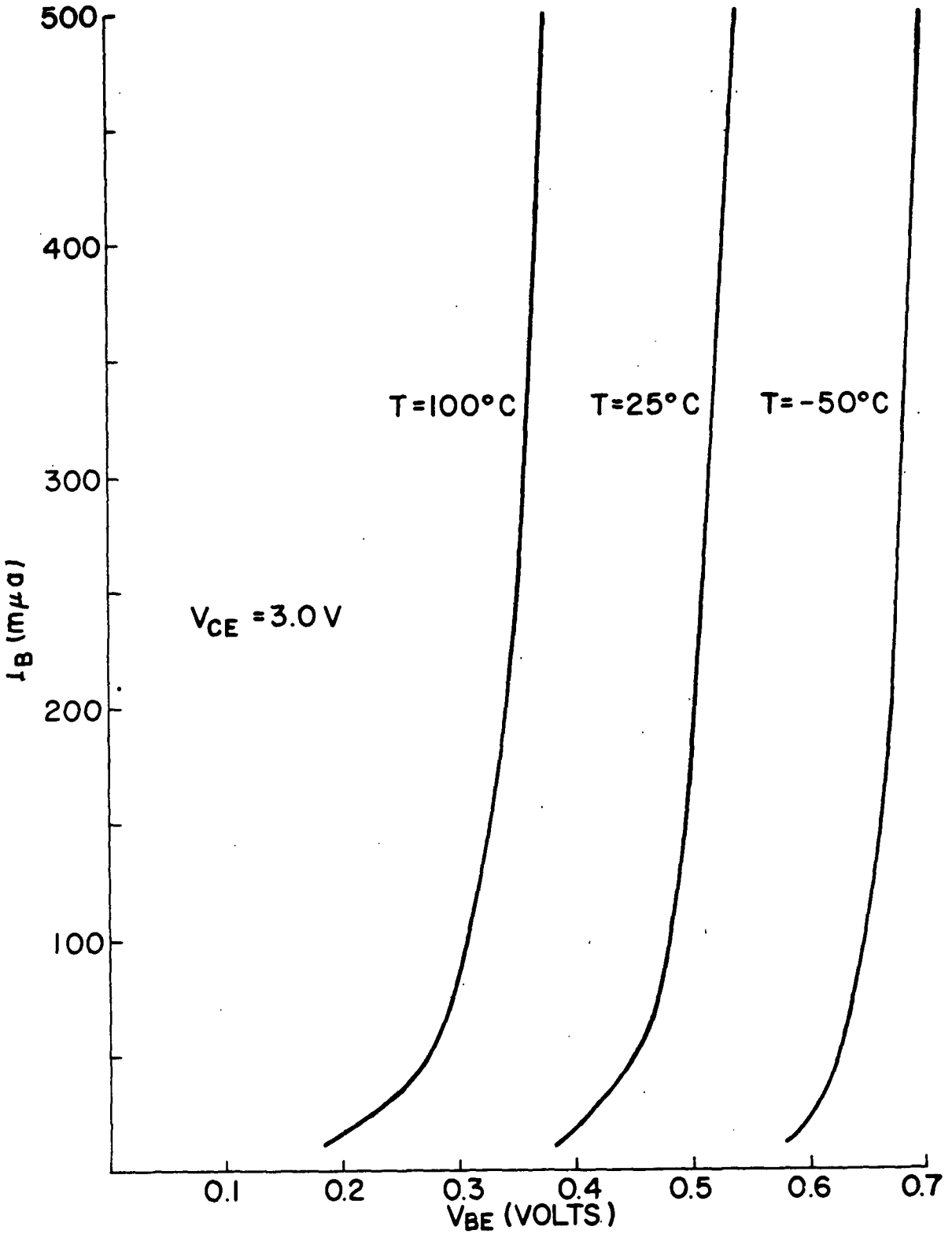


Figure 2 - Base Characteristics for Common Emitter Configuration; base current I_B versus base-to-emitter voltage V_{BE} for various operating temperatures T.

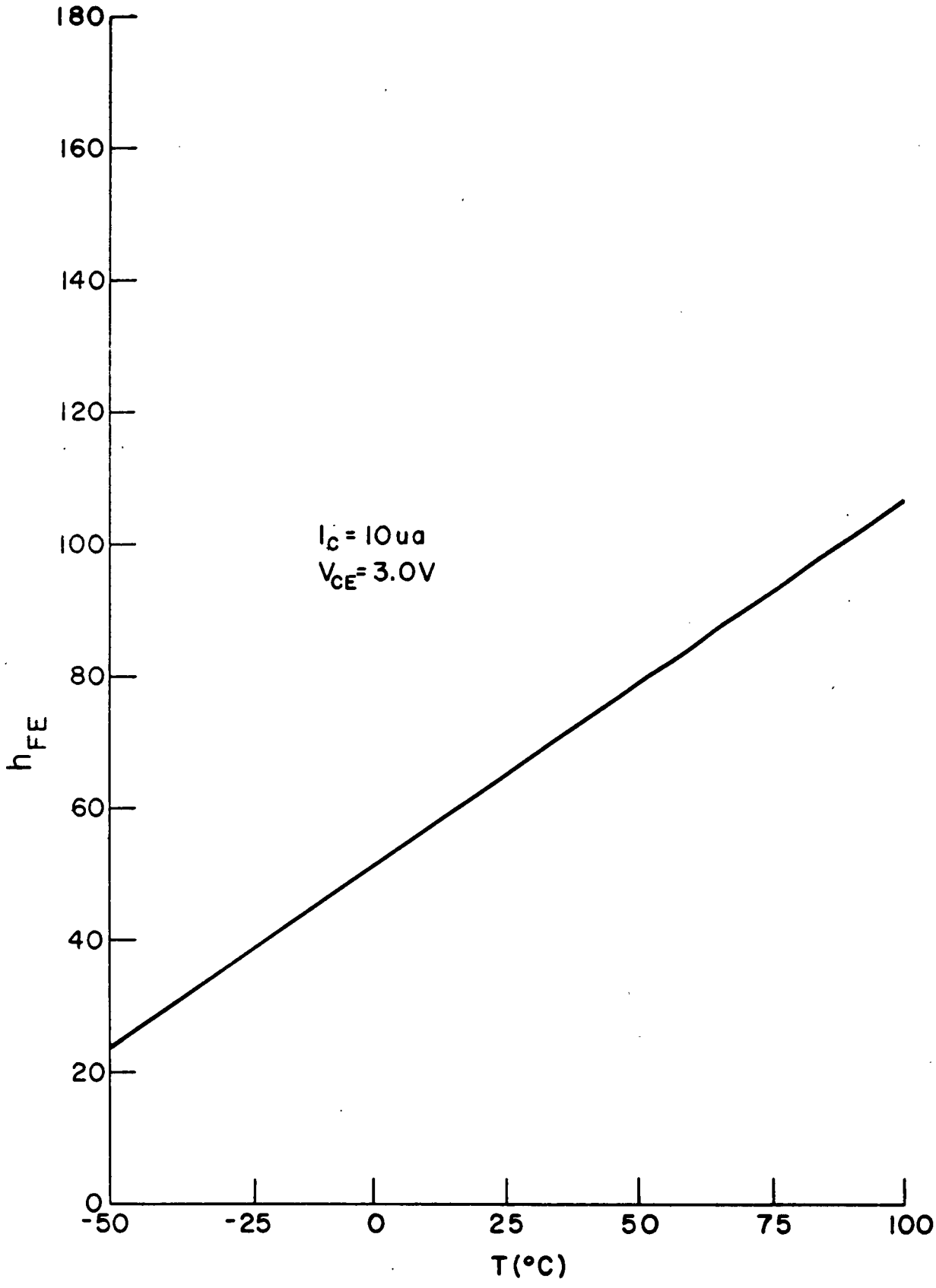


Figure 3 - Common emitter forward current transfer ratio h_{FE} versus temperature T.

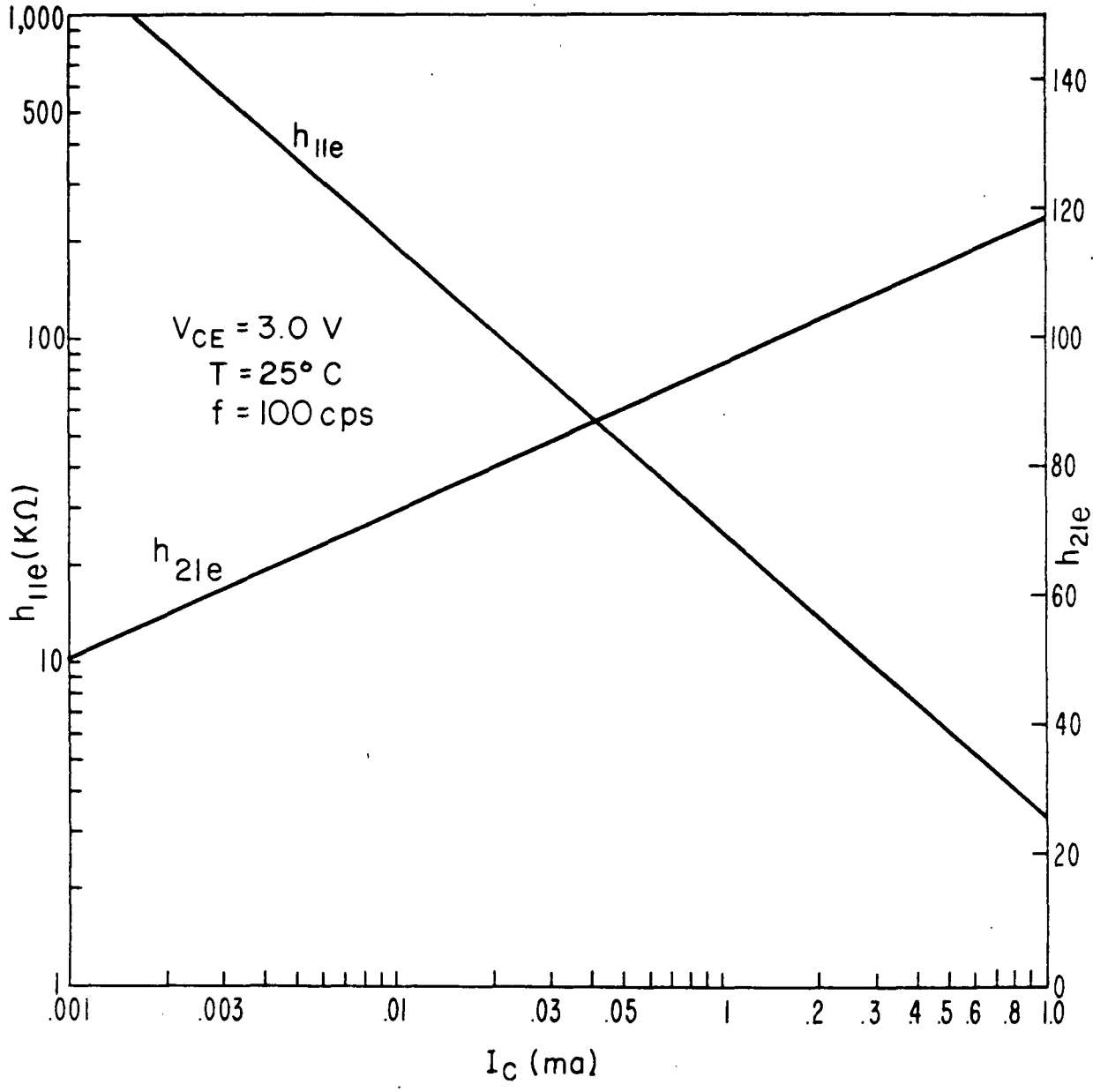


Figure 4 - Common emitter small-signal short-circuit input impedance $h_{ie} = h_{11e}$ and forward current transfer ratio $h_{fe} = h_{21e}$ versus collector current I_C.

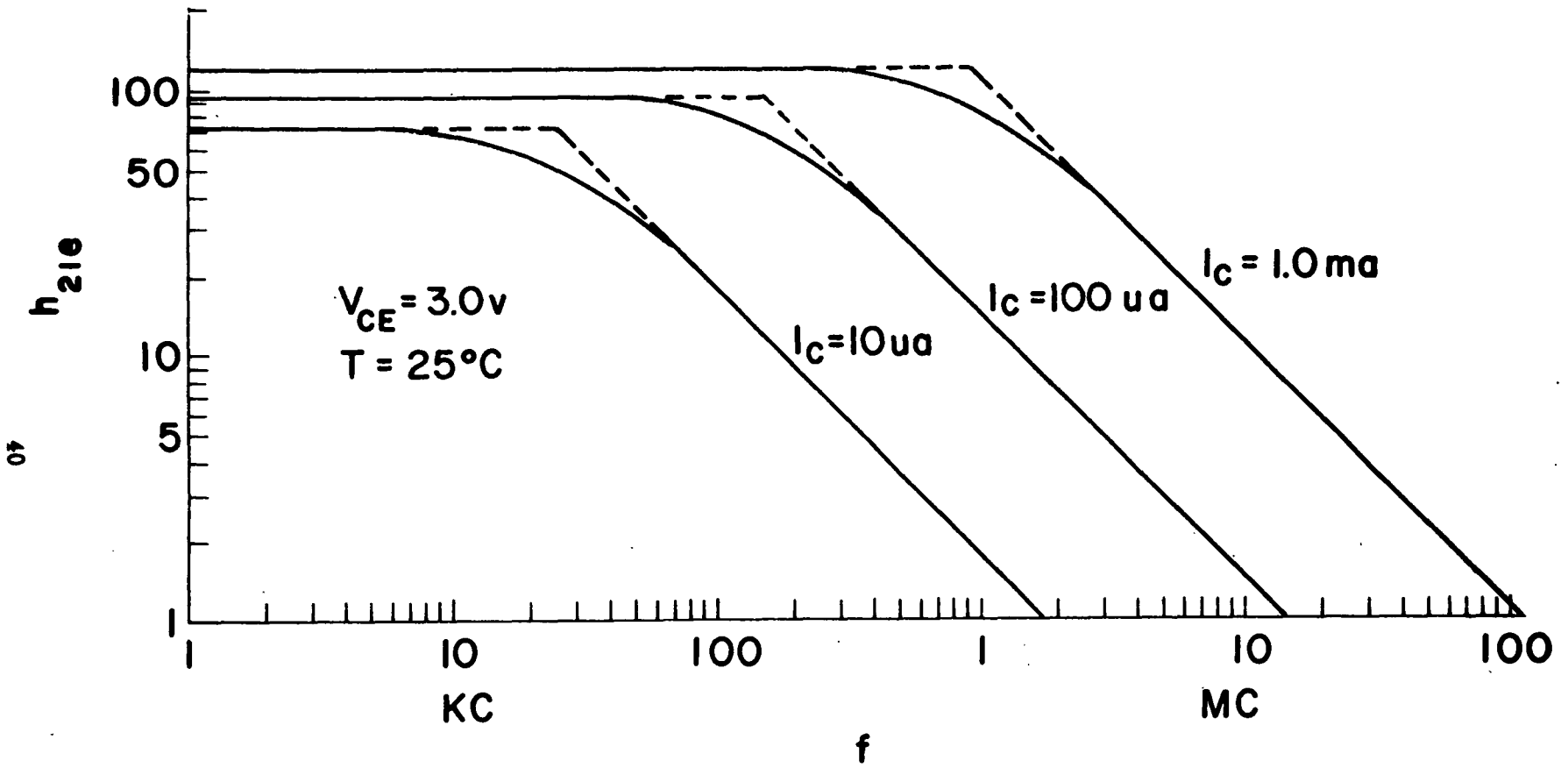


Figure 5 - Common emitter small-signal short-circuit forward current transfer ratio h_{21e} versus frequency f for various collector currents I_C.

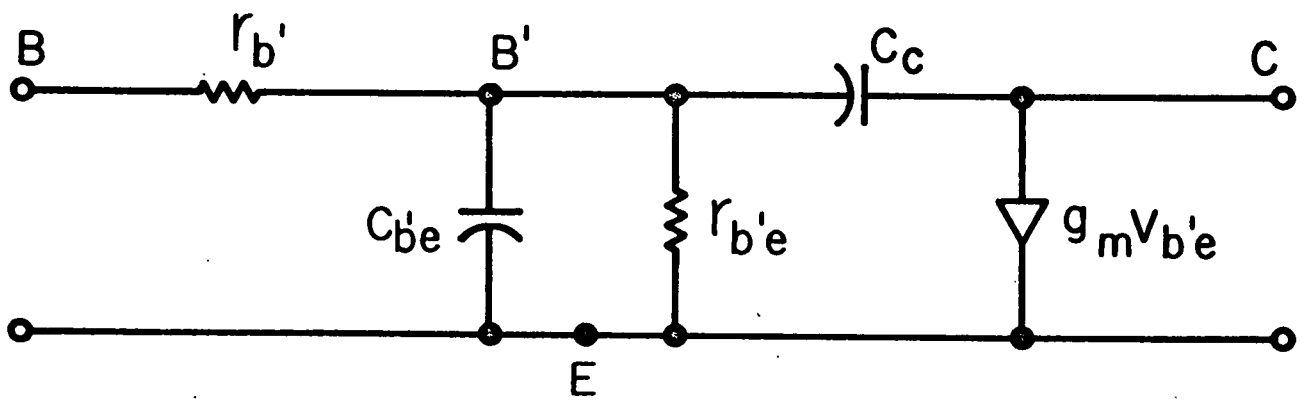


Figure 6 - Common emitter hybrid pi small-signal equivalent circuit for a micropower transistor.

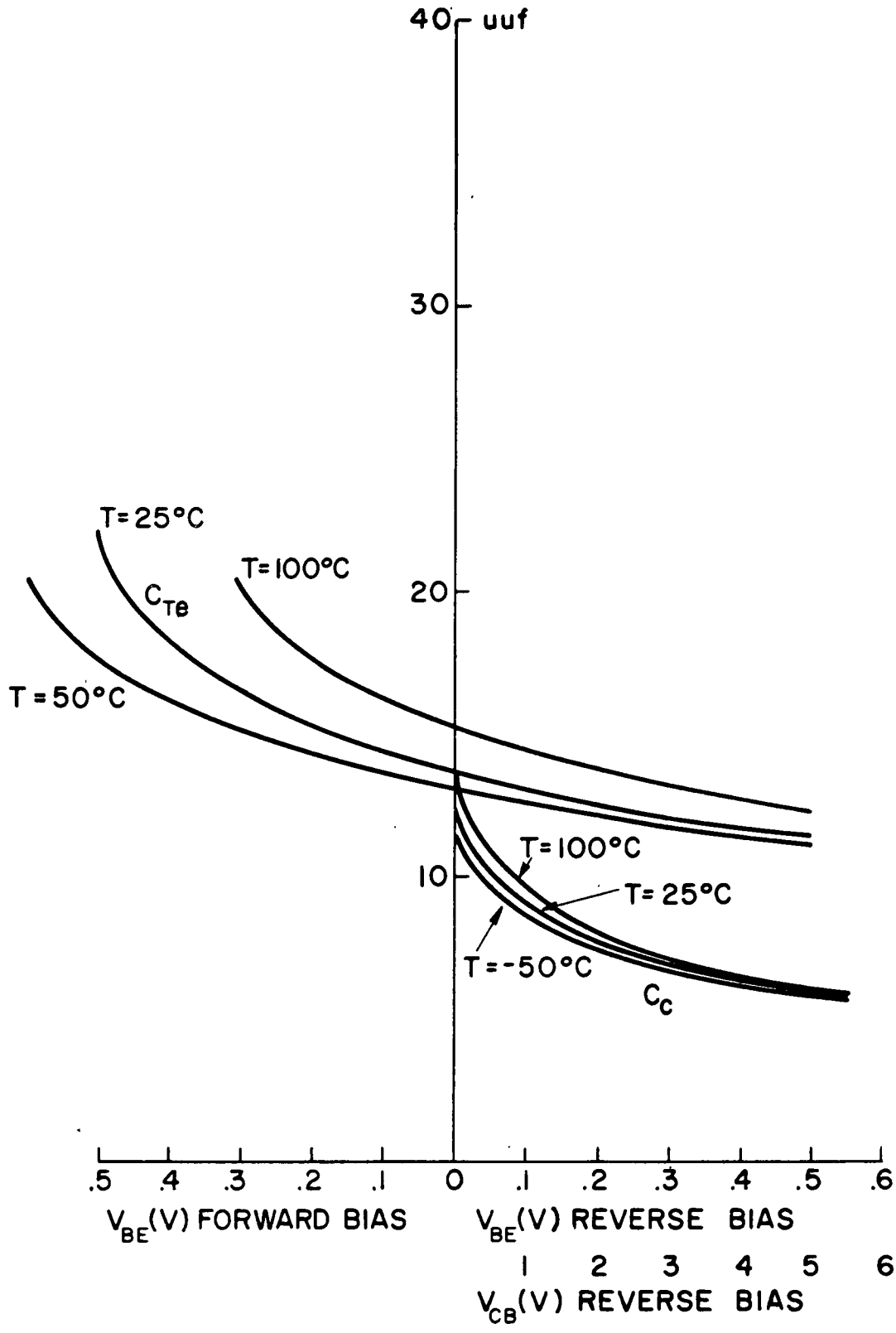


Figure 7 - Base-emitter junction capacitance C_{Te} versus base-to-emitter voltage V_{BE} and base-collector junction capacitance C_C versus collector-to-base voltage V_{CB} for various temperatures.

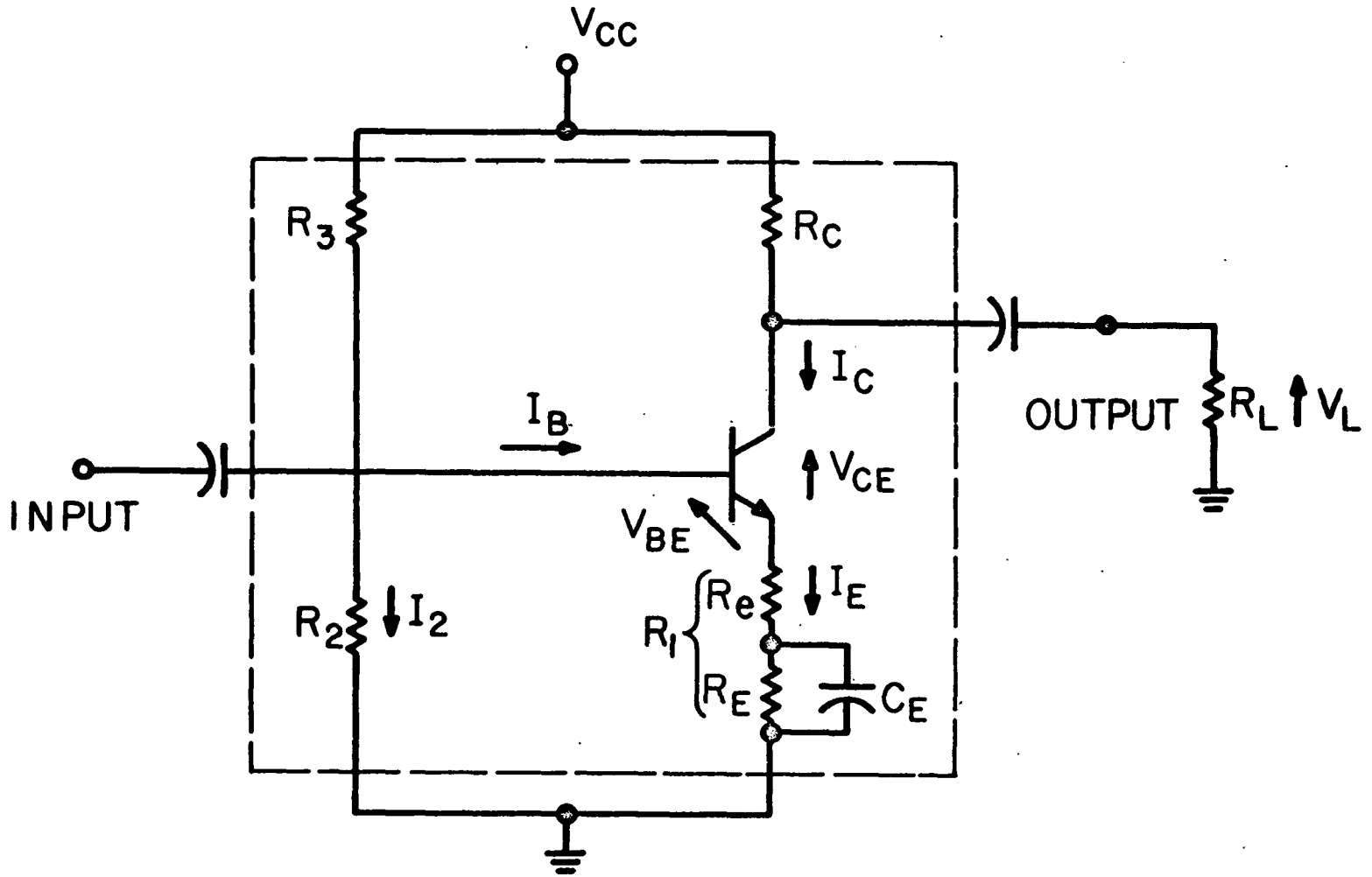


Figure 8 - Micropower amplifier schematic diagram indicating circuit DC currents and voltages and peak AC load voltage V_L.

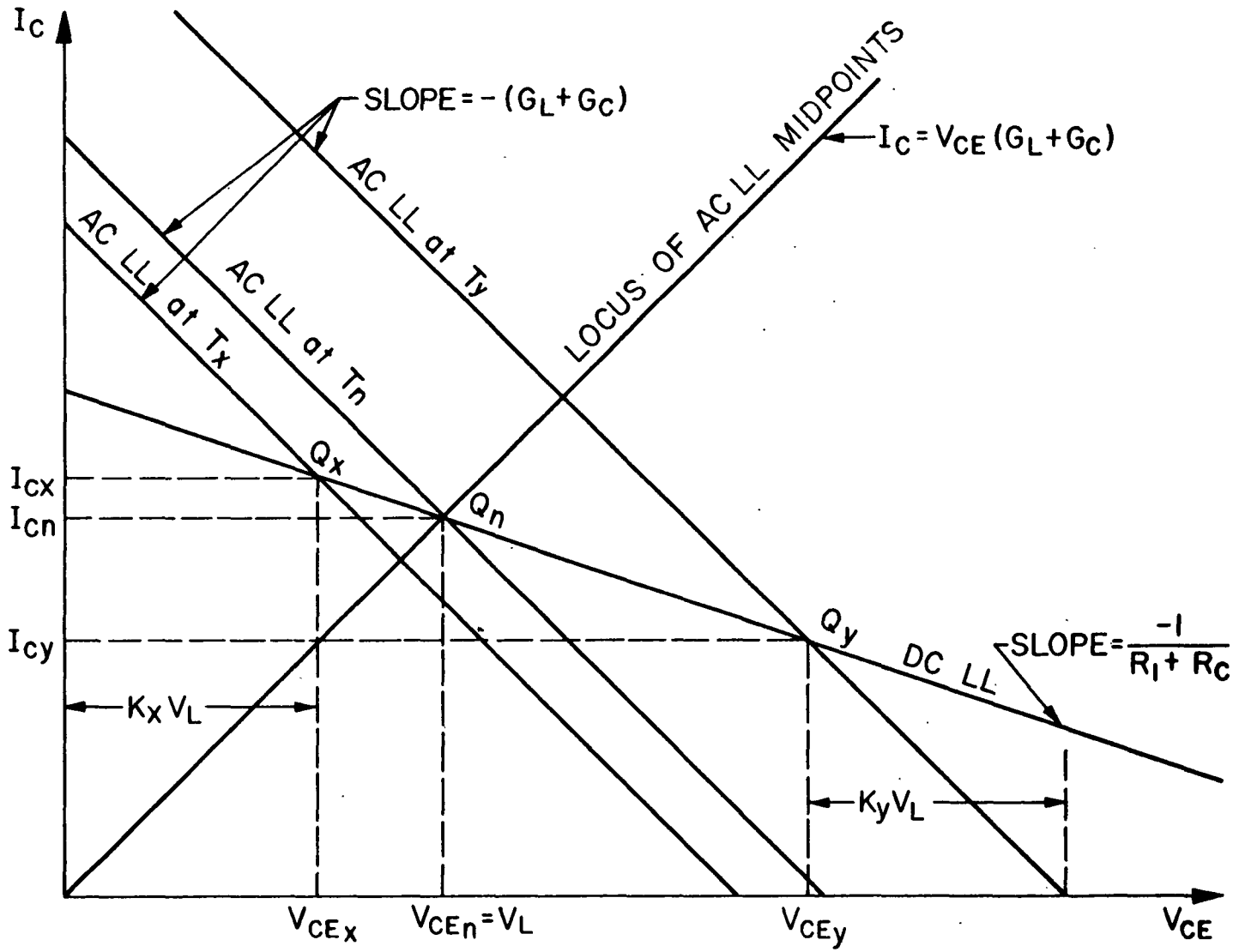


Figure 9 - Micropower amplifier load line diagram.

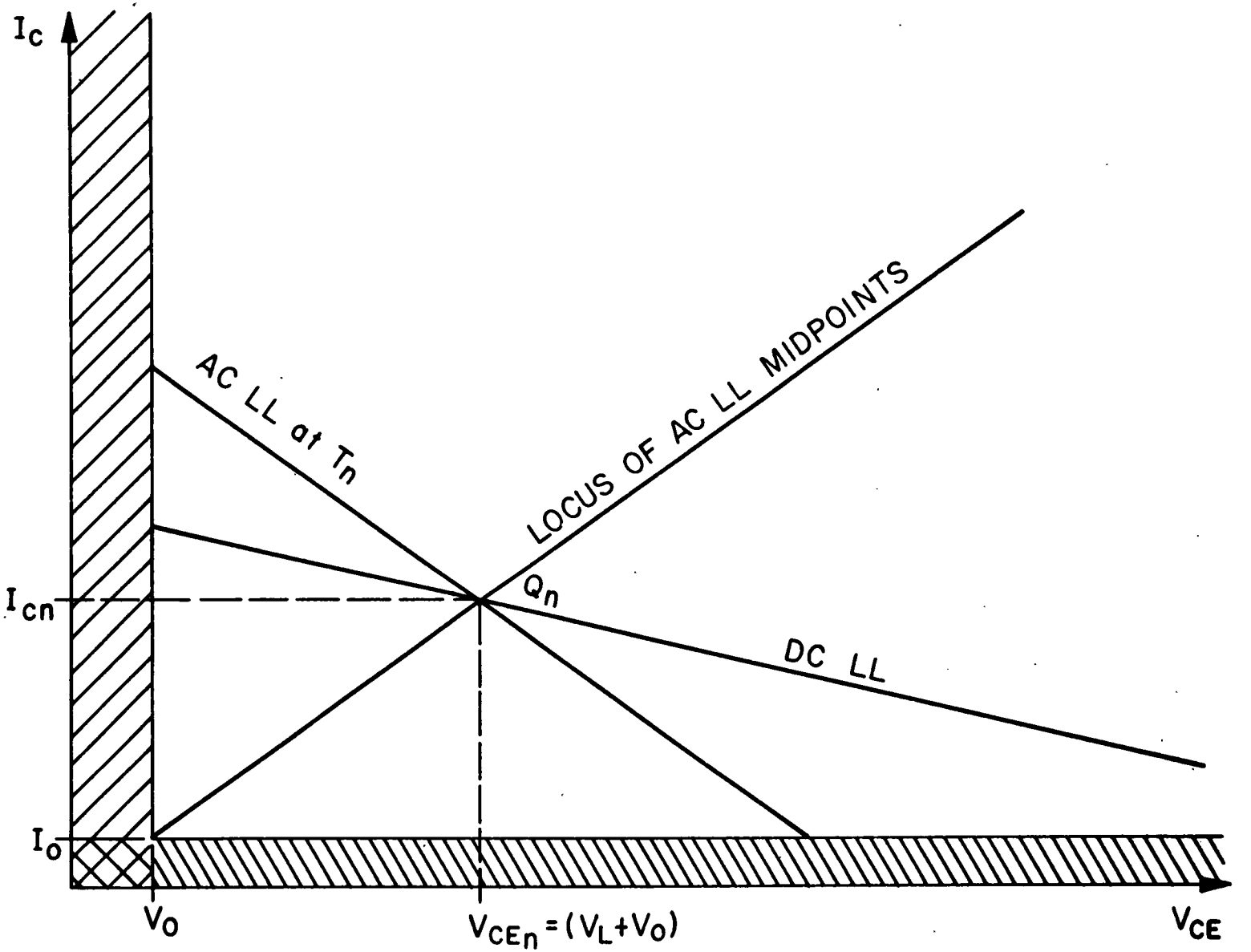


Figure 10 - Micropower amplifier load line diagram with offset regions.

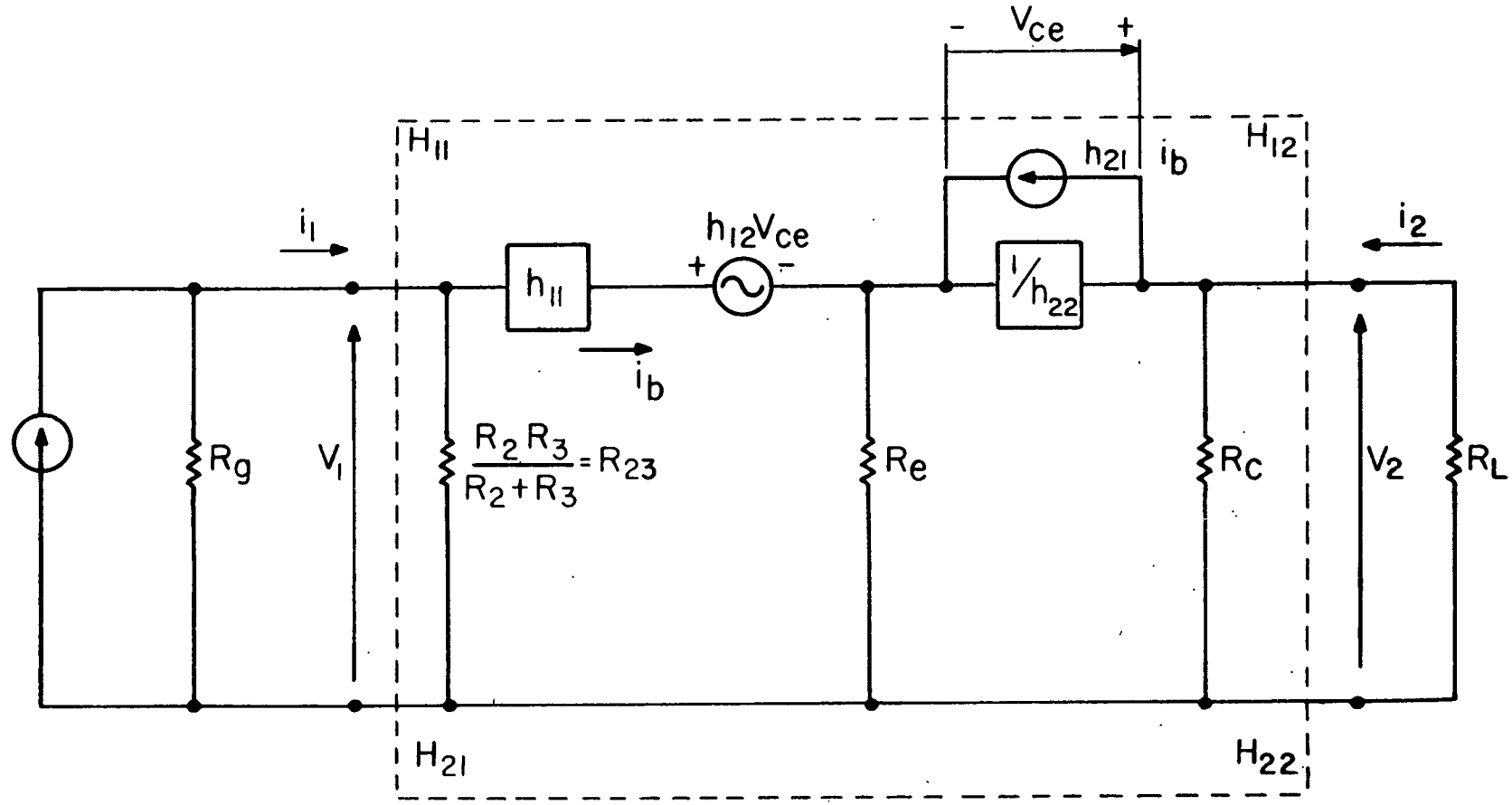


Figure 11 - Fourpole parameter representation of the small-signal AC equivalent circuit of a micropower amplifier.

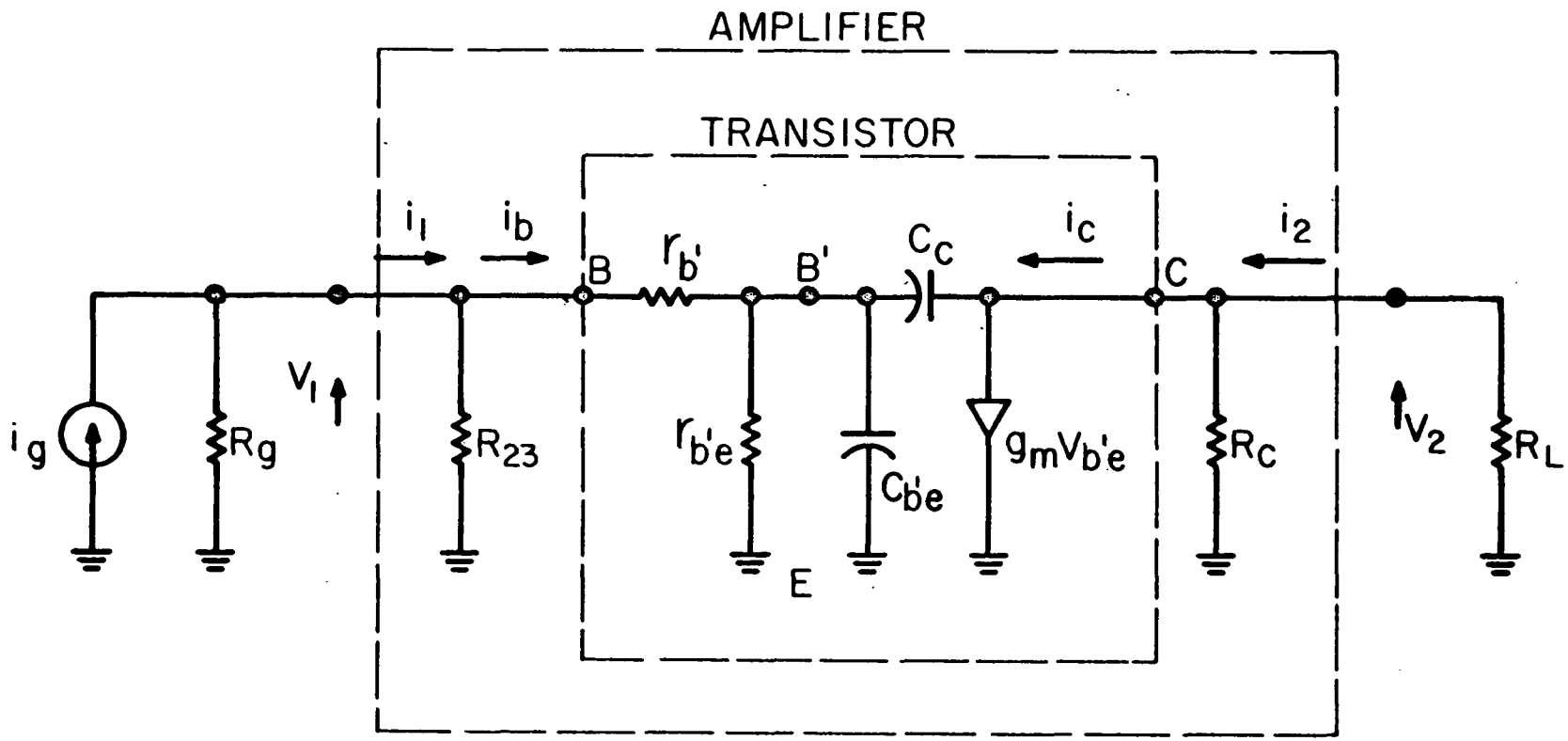


Figure 12 - Hybrid pi representation of the small-signal AC equivalent circuit of a micropower amplifier.

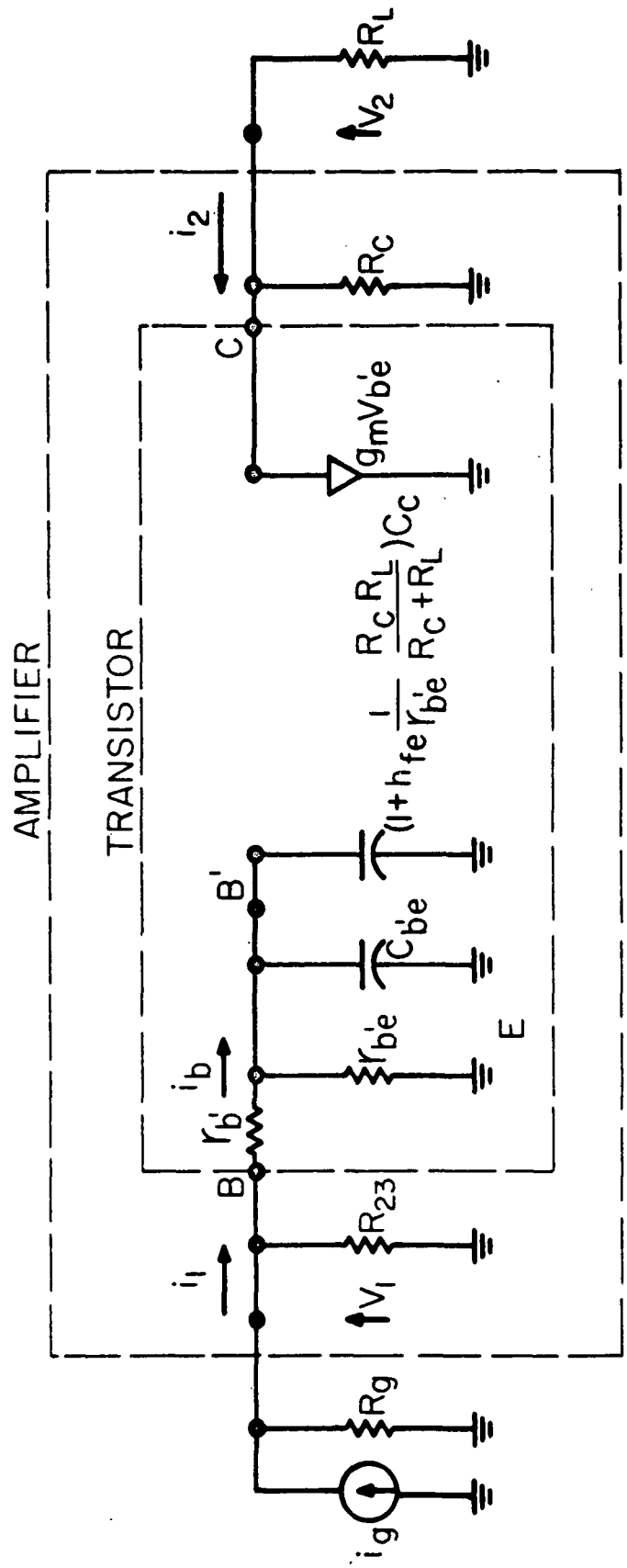


Figure 13 - Unilateralized hybrid pi equivalent circuit.

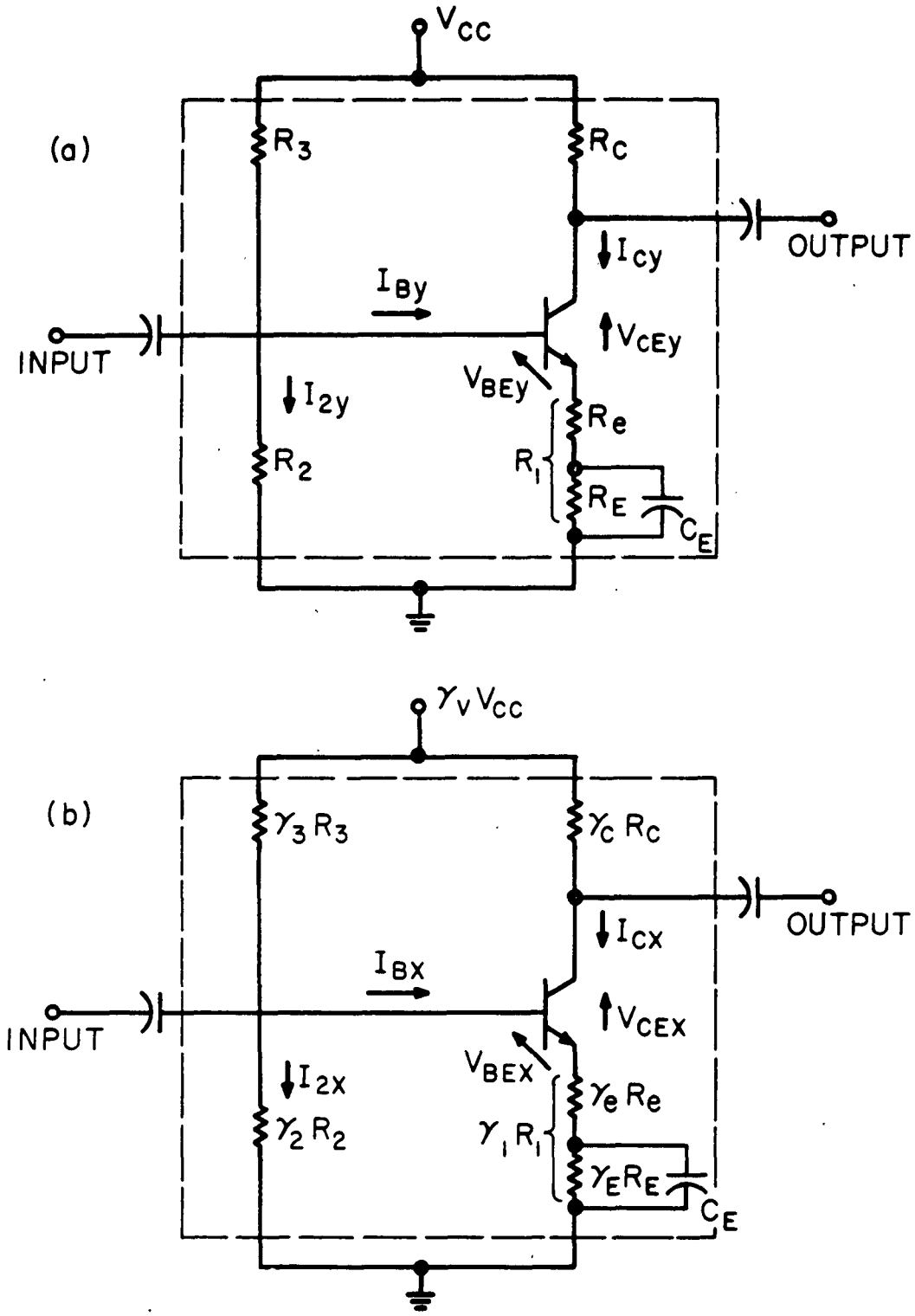
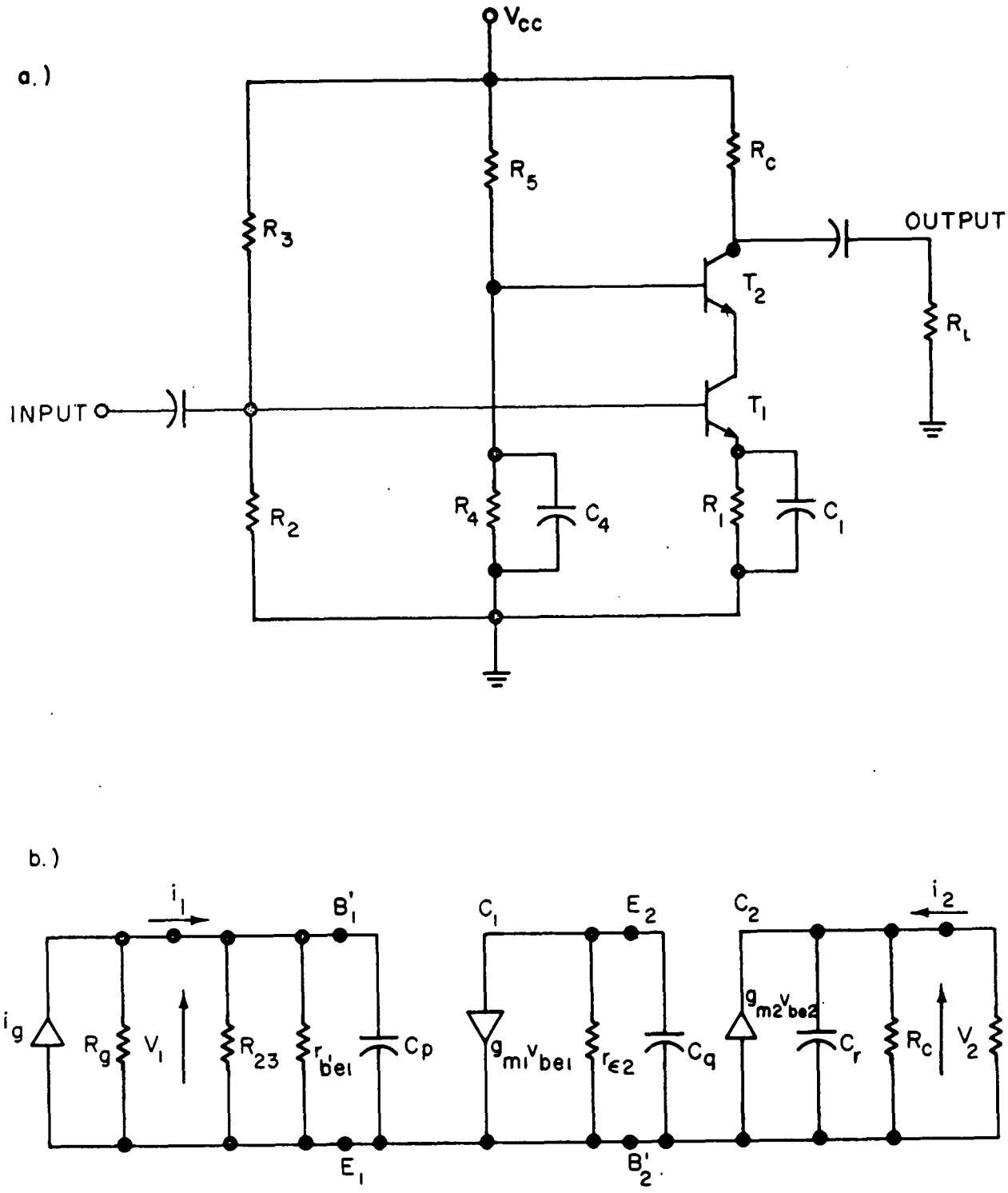


Figure 14 - Micropower amplifier schematic diagram indicating circuit currents, voltages and component values: (a) at the lower operating temperature limit T_y, and (b) at the upper operating temperature limit T_x.



$$C_p = C_{b'e1} + C_{b'es1} + (C_{c1} + C_{cs1})(1 + g_{m1} r_{\epsilon 2})$$

$$C_q = C_{b'e2} + C_{b'es2} + C_{ces1}$$

$$C_r = C_{c2} + C_{cs2}$$

Figure 15 - Cascode micropower amplifier (a) schematic diagram, (b) AC equivalent circuit.

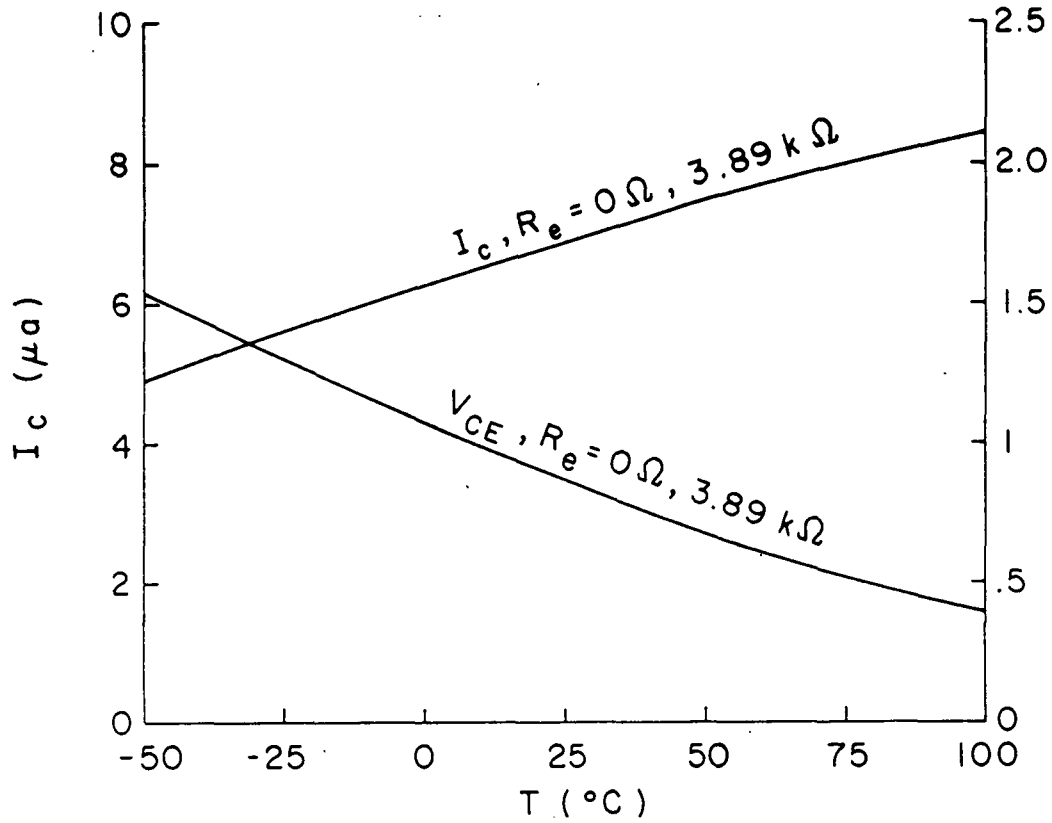


Figure 16 - Micropower amplifier quiescent collector current I_C and collector-to-emitter voltage V_{CE} versus temperature T.

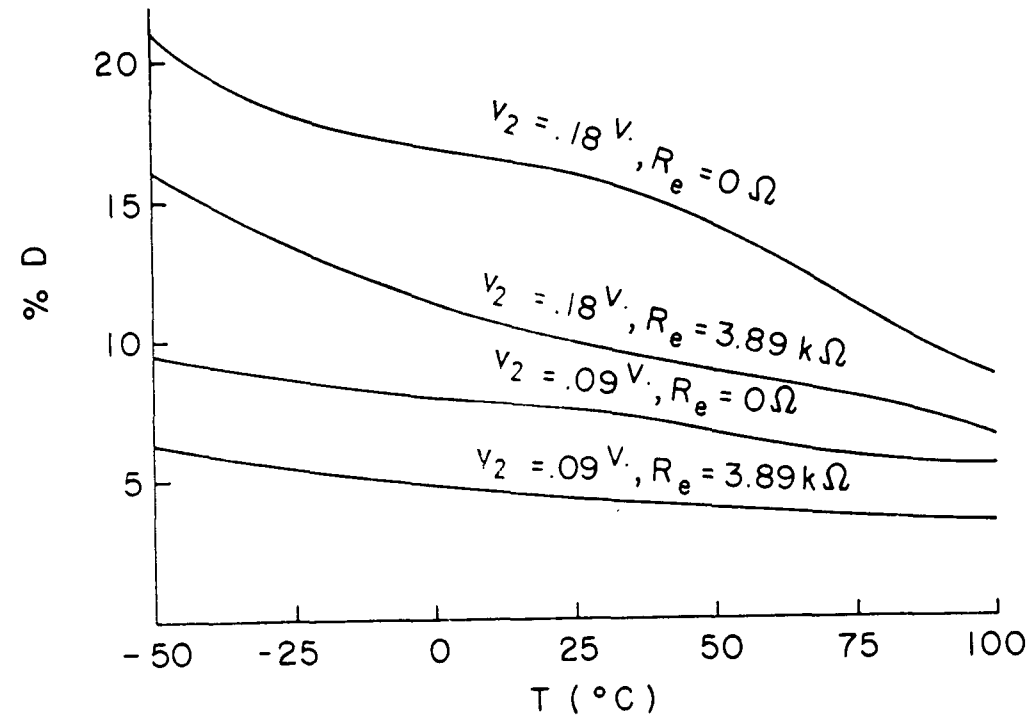


Figure 17 - Percent amplitude distortion in output waveform %D versus temperature T with AC emitter feedback resistance R_e=0, 3.89KΩ and peak output voltage swing V_L=0.18, 0.09 v.

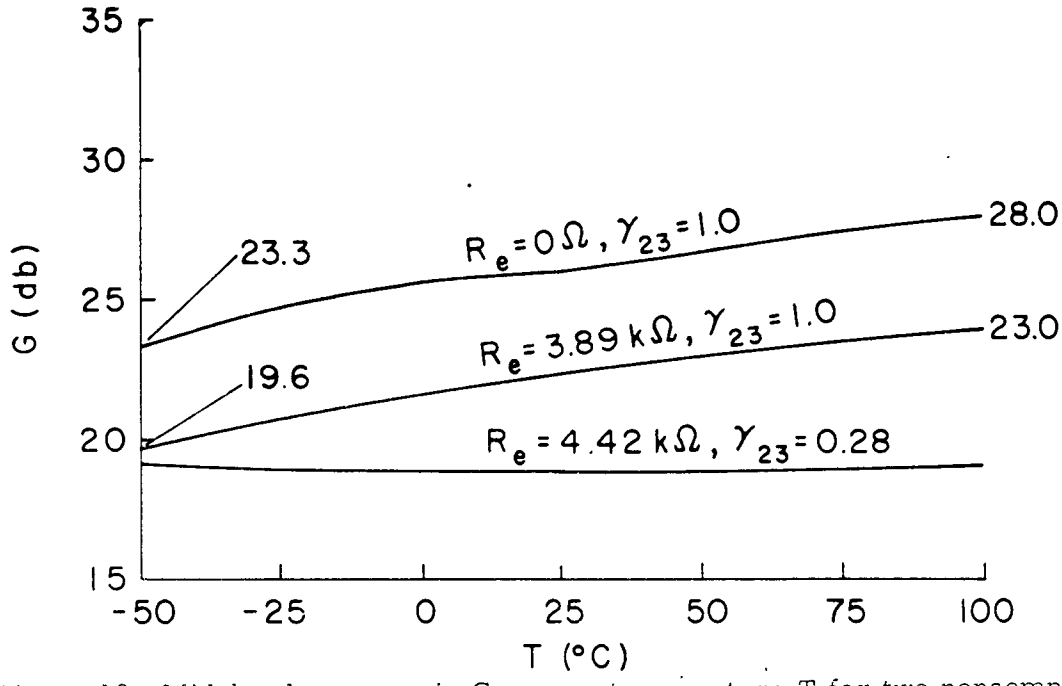


Figure 18 - Mid-band power gain G versus temperature T for two noncompensated amplifiers, R_e=0, γ_{23}=1.0 and R_e=3.89KΩ, γ_{23}=1.0 and a compensated amplifier R_e=4.42KΩ, γ_{23}=0.28.

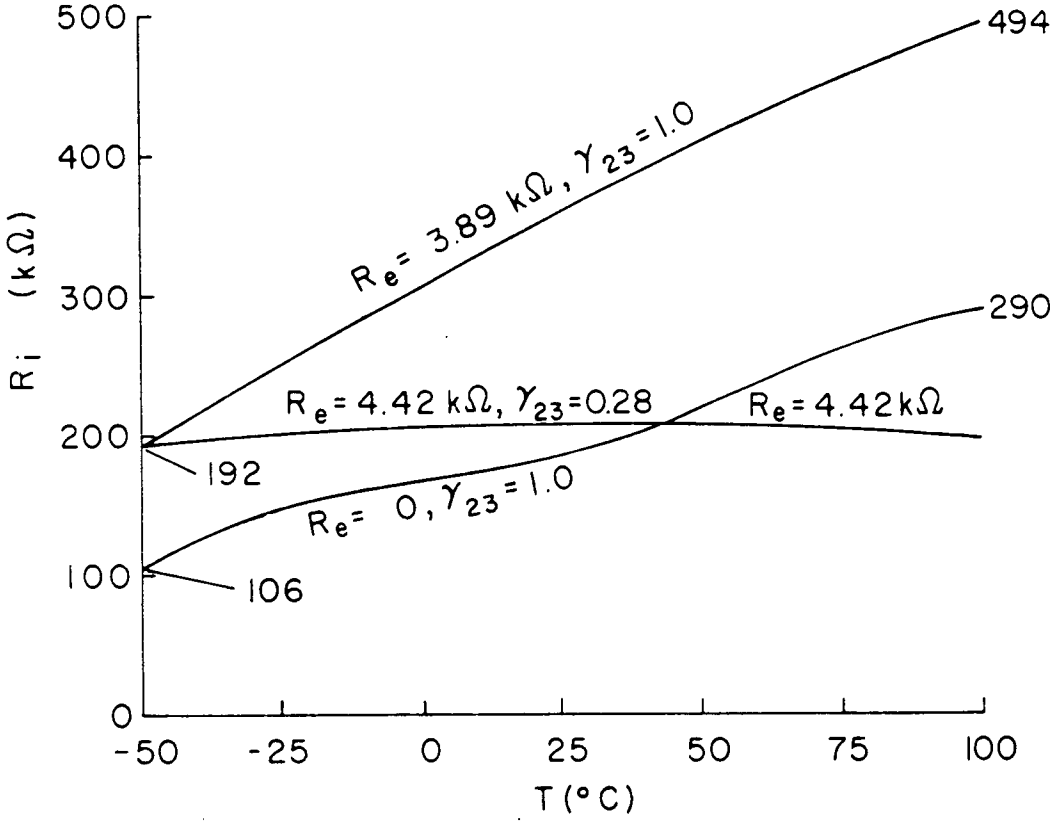


Figure 19 - Mid-band input impedance R_i versus temperature T for two noncompensated amplifiers, R_e=0, γ_{23}=1.0 and R_e=3.89KΩ, γ_{23}=1.0 and a compensated amplifier R_e=4.42KΩ, γ_{23}=0.28.

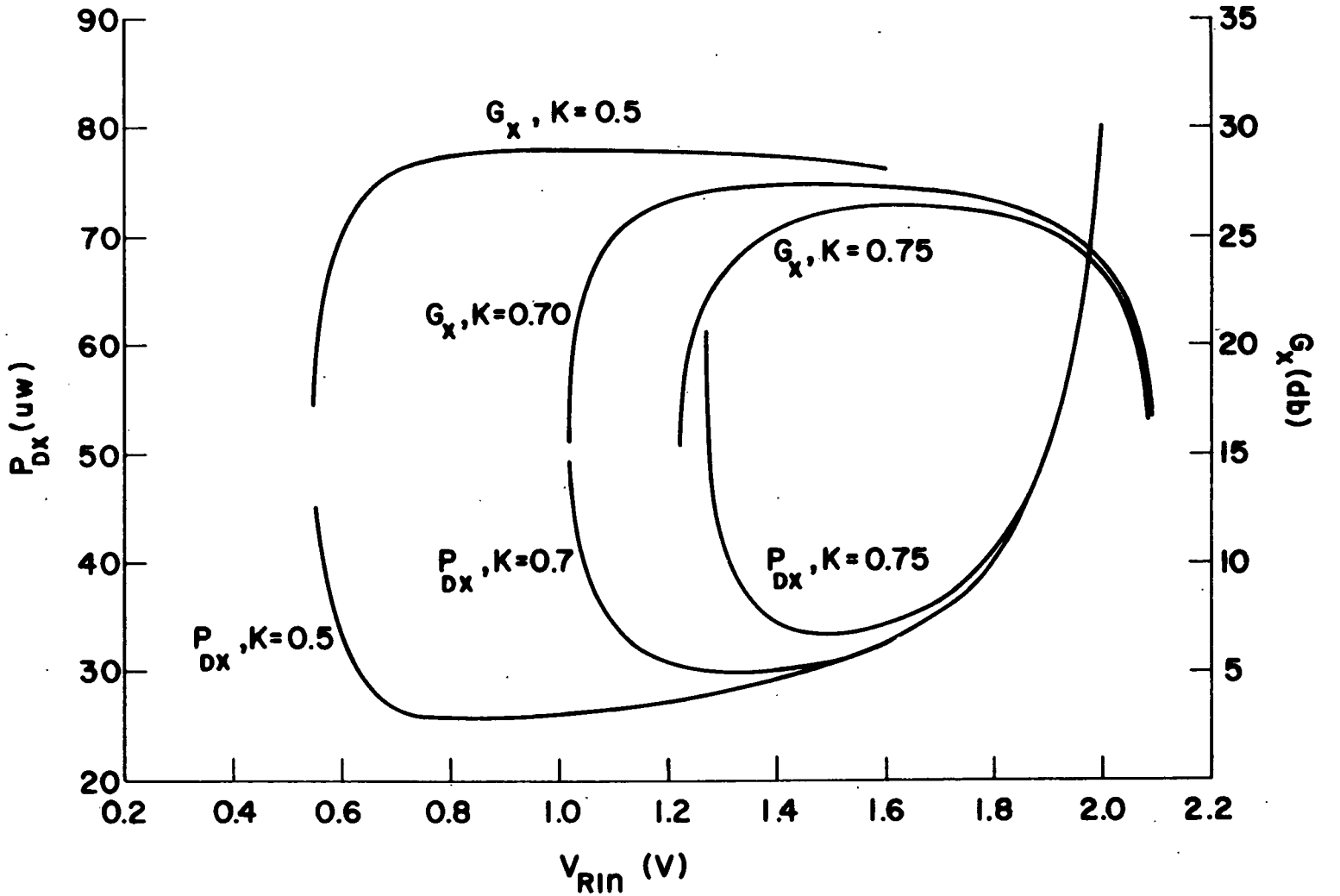


Figure 20 - Power gain G_X and power drain P_{DX} at upper temperature limit T_x versus DC emitter feedback voltage V_{RIn} at the nominal temperature T_n with dynamic range constant K=0.50, 0.70 and 0.75.

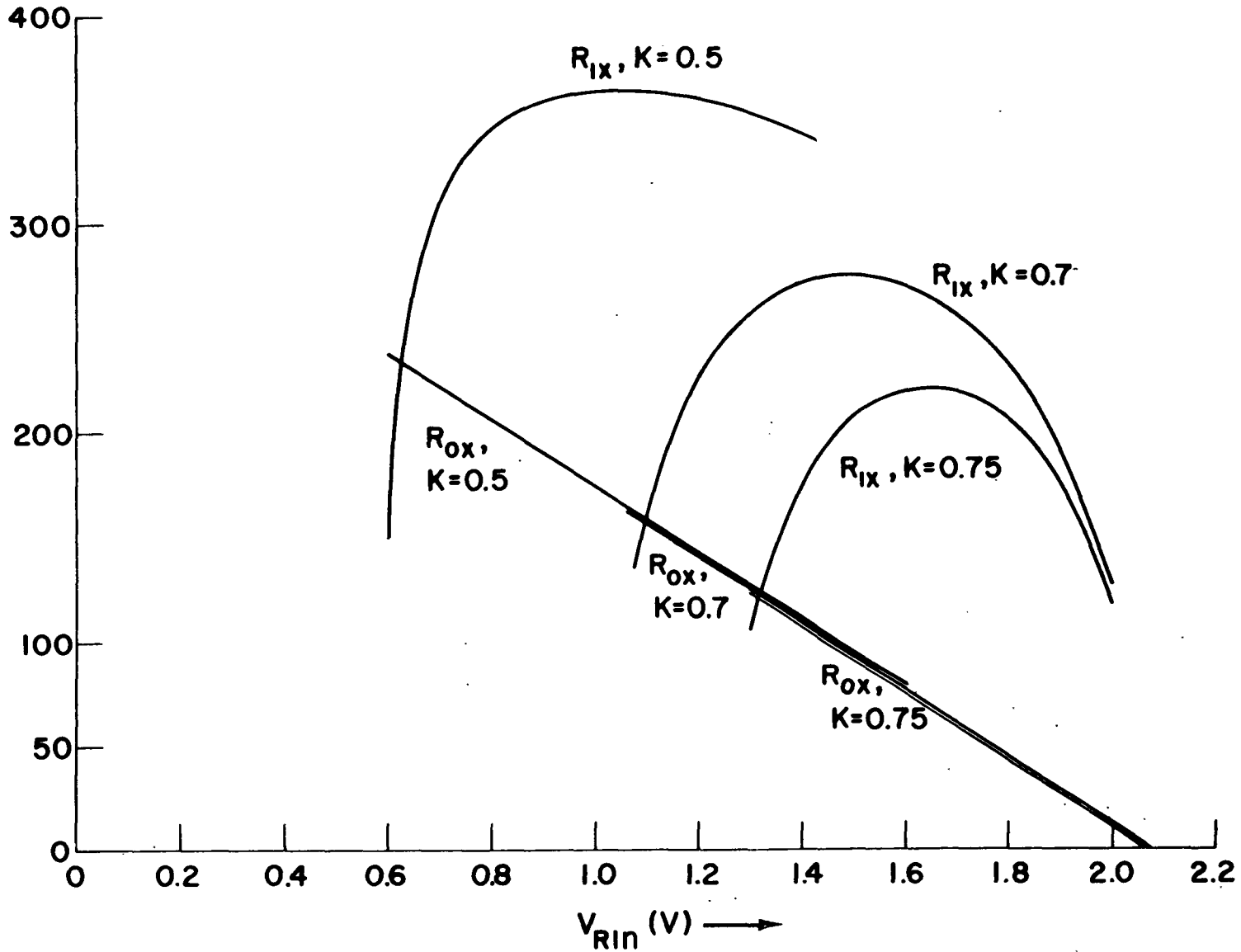


Figure 21 - Input impedance R_{ix} and output impedance R_{ox} at the upper temperature limit T_x versus DC emitter feedback voltage V_{RIn} at the nominal temperature T_n for dynamic range constant K=0.50, 0.70 and 0.75.

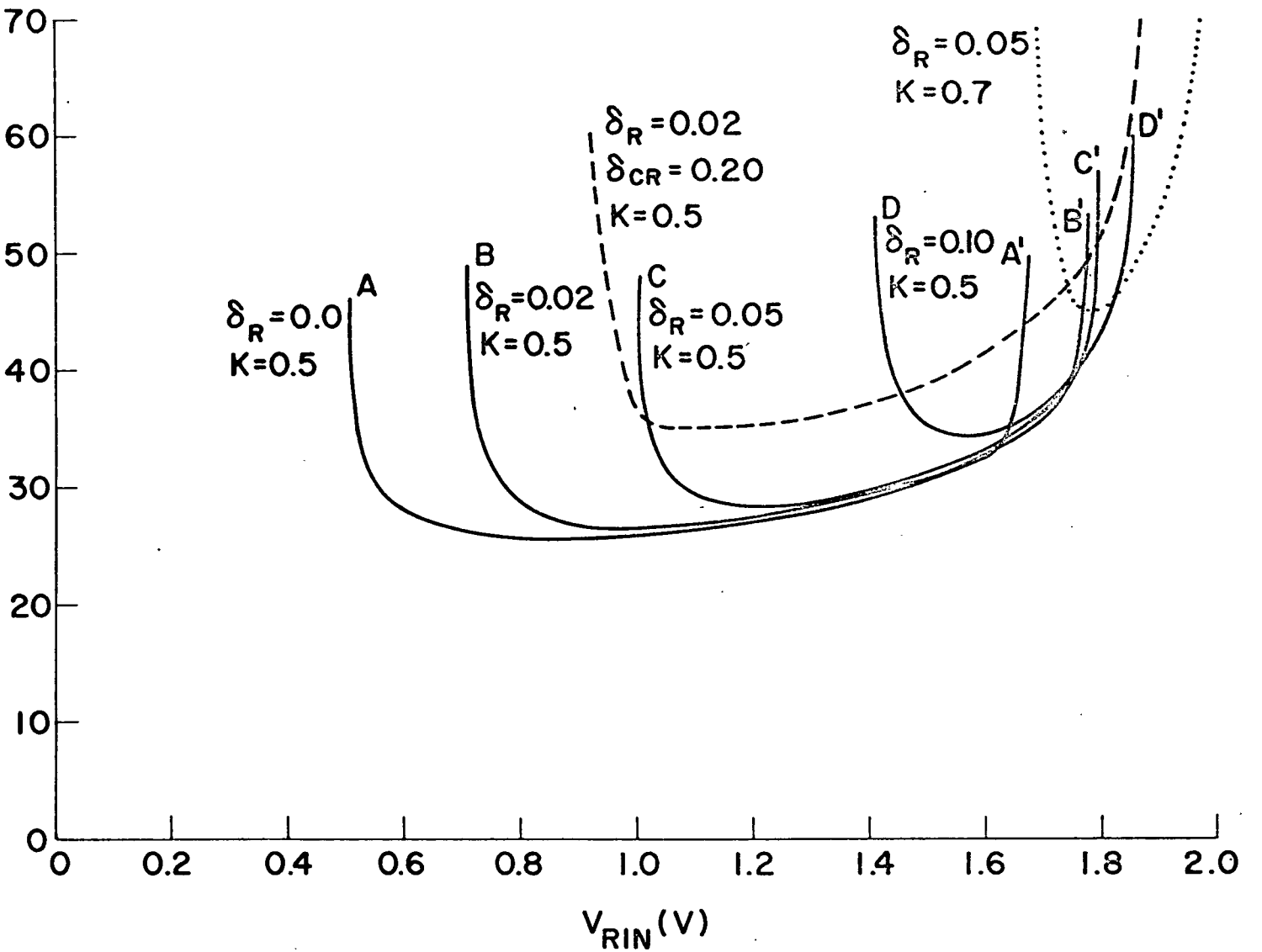


Figure 22 - Power drain P_{Dx} at upper temperature limit T_x versus DC emitter feedback voltage V_{R1n} at the nominal temperature T_n for various combinations of dynamic range constants K, worst case resistor tolerance δ_R and constant ratio resistor tolerance δ_{CR}.

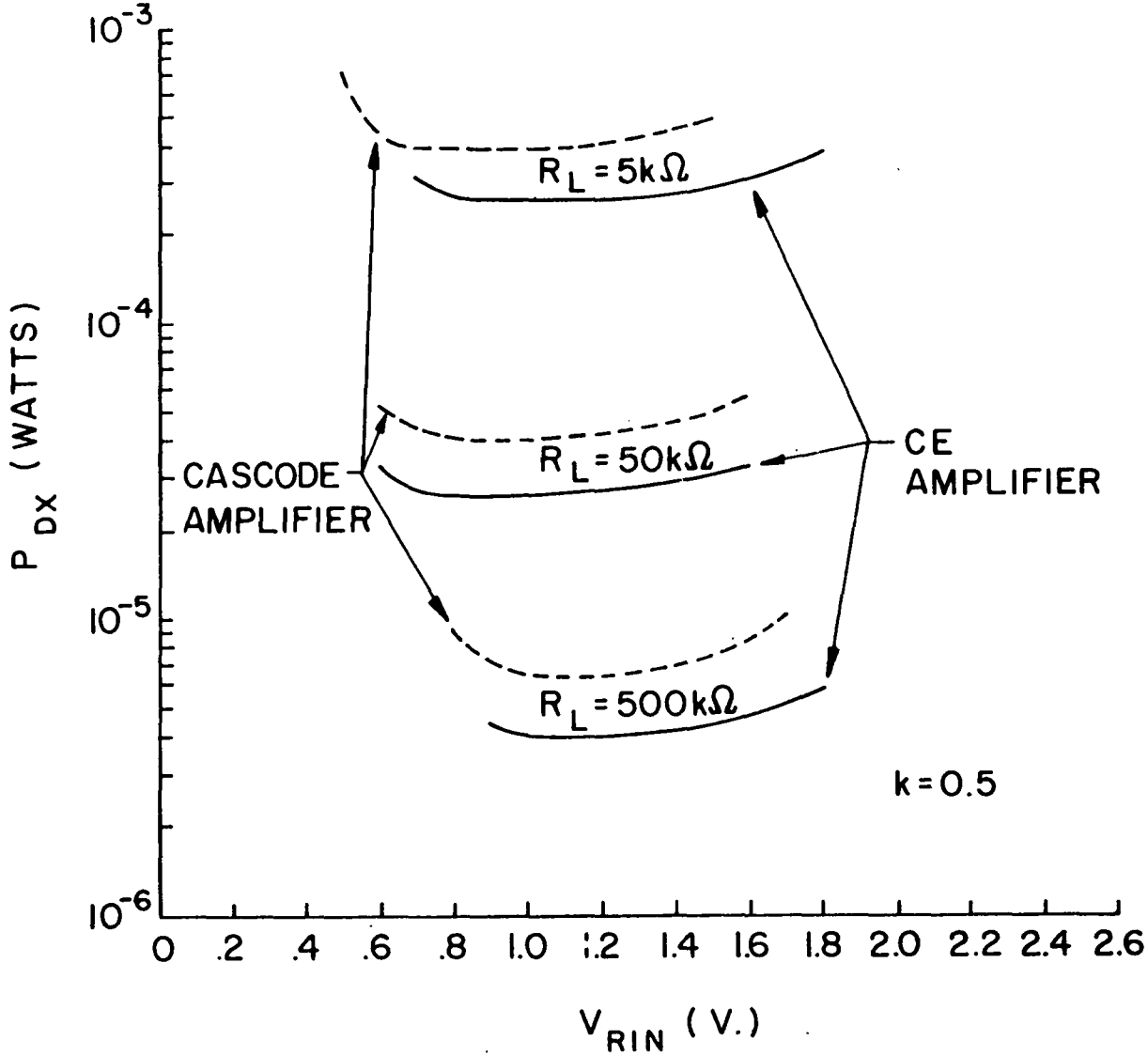


Figure 23 - Power drain P_{Dx} at upper temperature limit T_x versus DC emitter feedback voltage V_{RIn} at the nominal temperature T_n for the common emitter and the cascode amplifiers with various loads R_L.

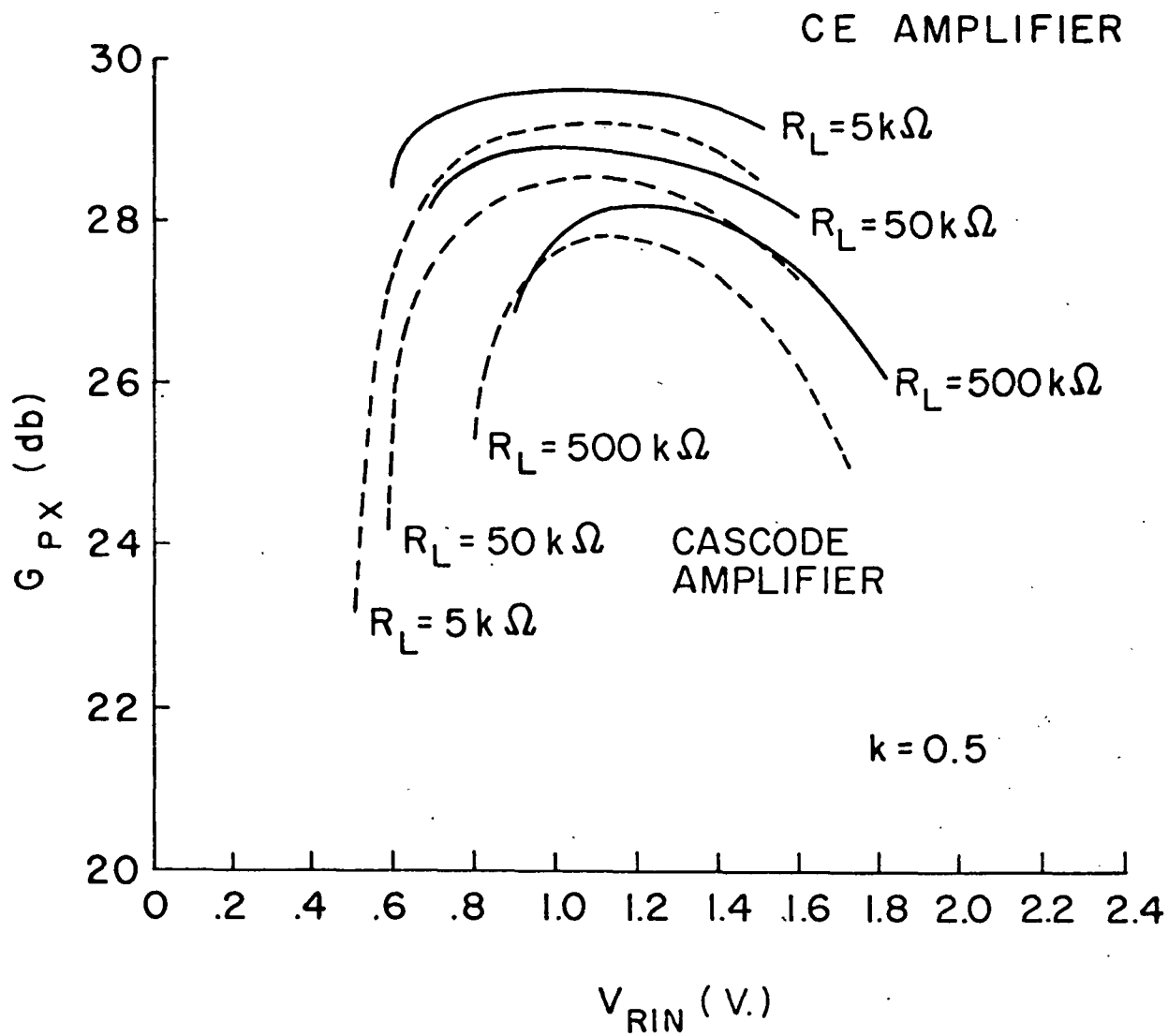


Figure 24 - Power gain G_x at upper temperature limit T_x versus DC emitter feedback voltage V_{R1n} at the nominal temperature T_n for the common emitter and the cascode amplifiers with various loads R_L.

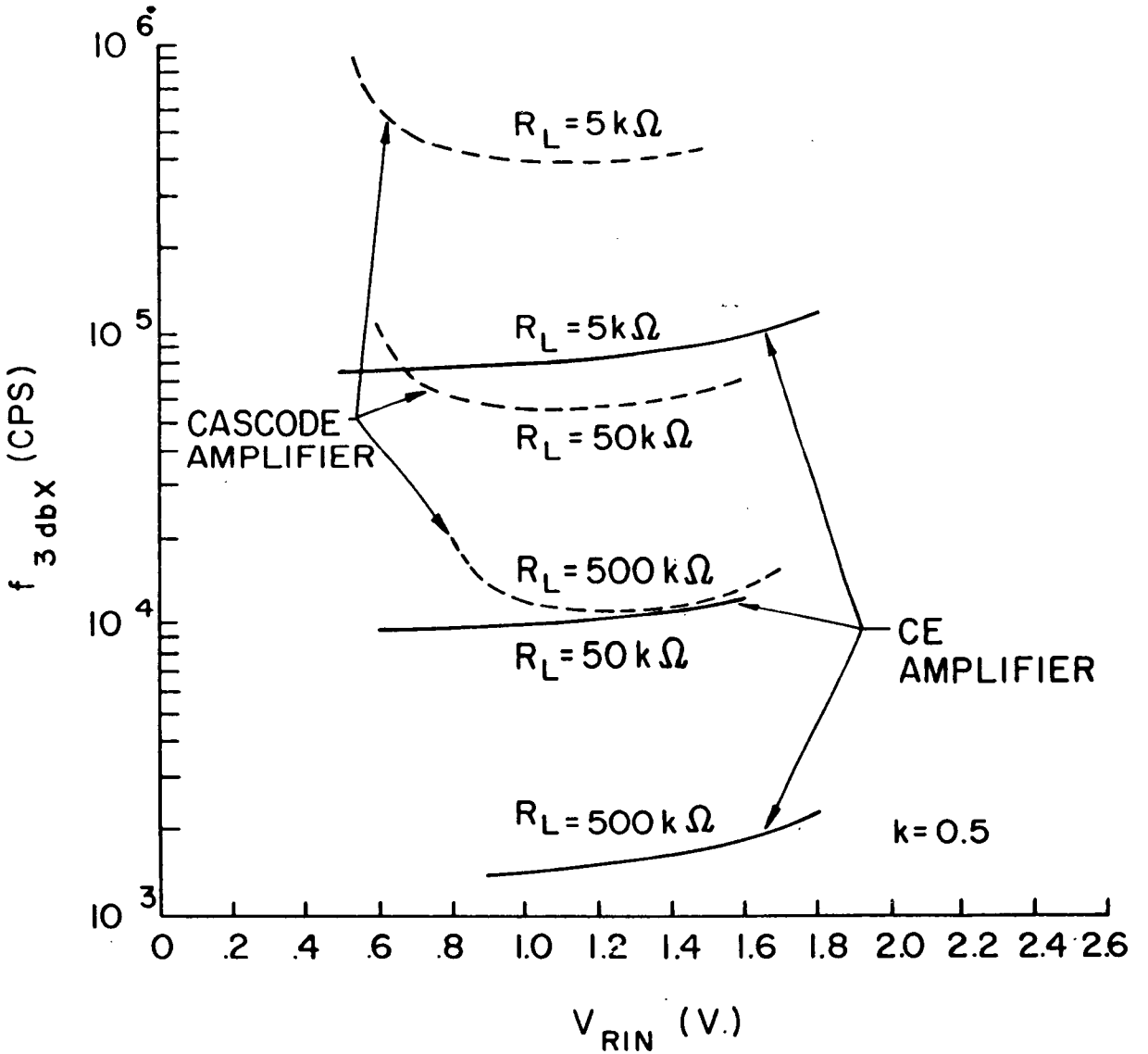


Figure 25 - Bandwidth ω_{3dbx} at upper temperature limit T_x versus DC emitter feedback voltage V_{R1n} at the nominal temperature T_n for the common emitter and the cascode amplifiers with various loads R_L.

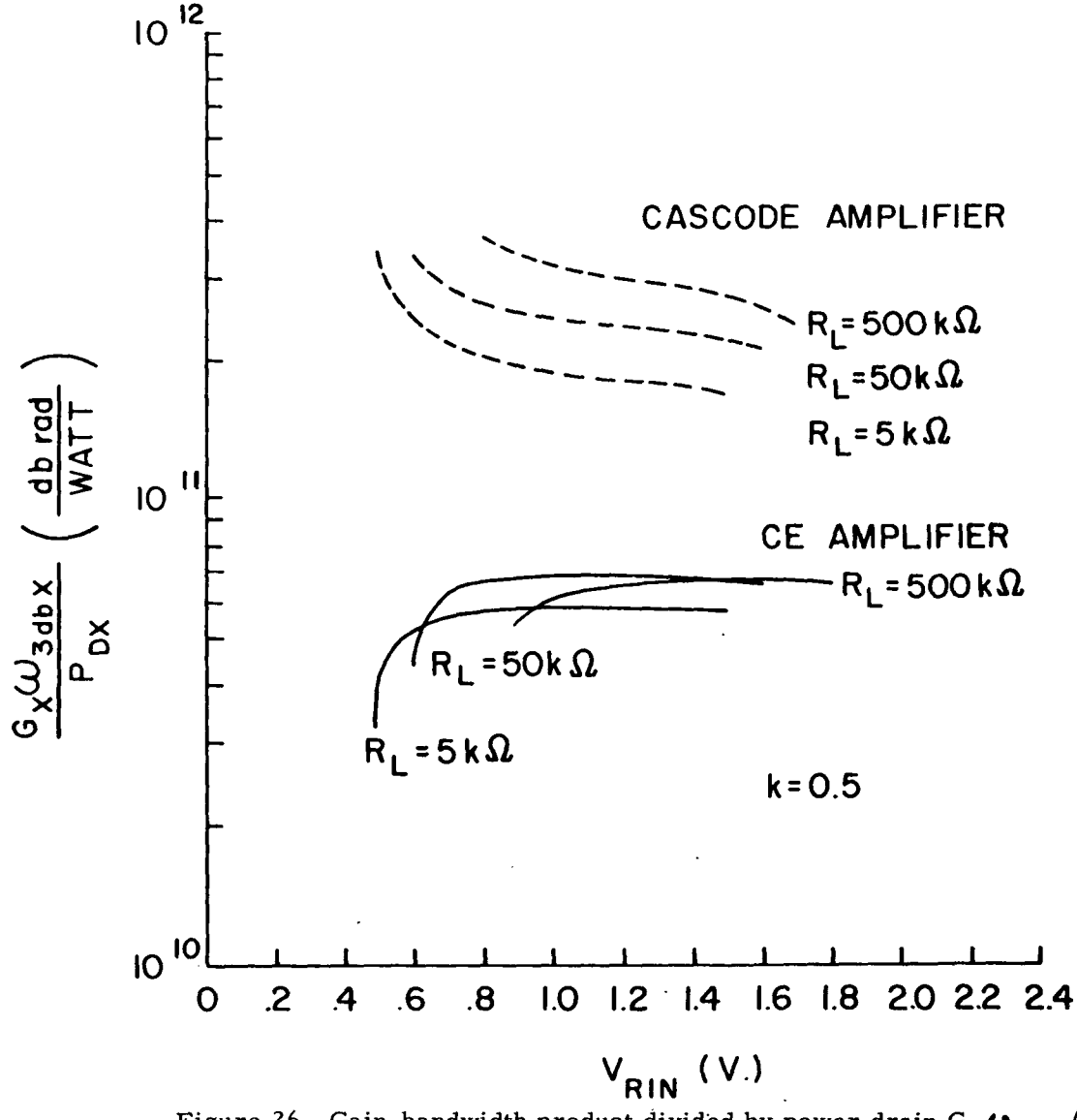


Figure 26 - Gain-bandwidth product divided by power drain $G_x \omega_{3dbx} / P_{Dx}$ at the upper temperature limit T_x versus DC emitter feedback voltage V_{R1n} at the nominal temperature T_n for the common emitter and the cascode amplifiers with various loads R_L.

DISTRIBUTION LIST

No. of Copies	Addressee
3	Commanding General U. S. Army Electronics Command Attn: AMSEL-AD Fort Monmouth, New Jersey
1	Office of the Assistant Secretary of Defense (Research and Engineering) Attn: Technical Library Room 3E1065, The Pentagon Washington 25, D. C.
2	Chief of Research and Development Department of the Army Washington 25, D. C.
1	Chief, United States Army Security Agency Attn: ACofS, G4(Technical Library) Arlington Hall Station Arlington 12, Virginia
1	Commanding Officer U.S. Army Electronics Research and Development Activity Attn: Technical Library Fort Huachuca, Arizona
1	Commanding Officer U. S. Army Electronics Research and Development Activity ATTN: SELWS-AJ White Sands, New Mexico 88002
1	Commanding Officer U. S. Army Electronics Research Unit P.O. Box 205 Mountain View, California
1	Commanding Officer U.S. Army Electronics Materiel Support Agency (Attn: SELMS-ADJ) Fort Monmouth, New Jersey
1	USAELRDL Liaison Officer U. S. Army Combat Developments Command CDCLN-EL Fort Belvoir, Virginia
1	Commanding Officer Engineer Research and Development Laboratories Attn: Technical Documents Center Fort Belvoir, Virginia
1	Commanding Officer U. S. Army Chemical Warfare Laboratories Attn: Technical Library, Bldg. 330 Army Chemical Center Maryland
1	Commanding Officer Harry Diamond Laboratories Attn: Library, Bldg. 92 Room 211 Washington 25, D. C.
2	Headquarters, U. S. Air Force Attn: AFCIN Washington 25, D. C.
1	Rome Air Development Center Attn: RAALD Griffiss Air Force Base New York
1	Headquarters Ground Electronics Engineering Installation Agency Attn: ROZMEL Griffiss Air Force Base New York

DISTRIBUTION LIST (Cont)

No. of Copies	Addressee
2	Commanding General U.S. Army Materiel Command Attn: R&D Directorate Washington 25, D. C.
1	Aeronautical Systems Div. Attn: ASNXRR Wright-Patterson Air Force Base, Ohio
1	U.S. Air Force Security Service Attn: ESD San Antonio, Texas
1	Headquarters Strategic Air Command Attn: DOCE Offutt Air Force Base, Nebraska
1	Headquarters Research & Technology Div. Attn: RTH Bolling Air Force Base Washington 25, D. C.
1	Air Proving Ground Center Attn: PGAPI Eglin Air Force Base, Florida
2	Air Force Cambridge Research Laboratories Attn: CRXL-R L.G. Hanscom Field Bedford, Massachusetts
2	Headquarters Electronic Systems Div. Attn: ESAT L.G. Hanscom Field Bedford, Massachusetts
1	Chief of Naval Research Attn: Code 427 Department of the Navy Washington 25, D. C.
1	Bureau of Ships Technical Library Attn: Code 312 Main Navy Bldg., Room 1528 Washington 25, D. C.
1	Chief, Bureau of Ships Attn: Code 454 Department of the Navy Washington 25, D. C.
1	Chief, Bureau of Ships Attn: Code 686B Department of the Navy Washington 25, D. C.
1	Director U.S. Naval Research Laboratory Attn: Code 2027 Washington, D. C. 20390
1	Commanding Officer & Director U.S. Navy Electronics Lab. Attn: Library San Diego 52, California
1	Commander U. S. Naval Ordnance Laboratory White Oak Silver Spring 19, Maryland
20	Commander Defense Documentation Center Attn: TISIA Cameron Station, Bldg, 5 Alexandria, Virginia 22314

DISTRIBUTION LIST (Cont)

No. of Copies	Addressee
1	AFSC Scientific/Technical Liaison Office U.S. Naval Air Development Center Johnsville, Pennsylvania
1	USAELRDL Liaison Officer U.S. Naval Research Laboratory Attn: Code 1071 Washington, D. C. 20390
1	USAELRDL Liaison Officer Massachusetts Institute of Technology Building 26, Room 131 77 Massachusetts Avenue Cambridge 39, Massachusetts
1	USAELRDL Liaison Office Aeronautical Systems Division Attn: ASDL-9 Wright-Patterson Air Force Base, Ohio
1	U.S. Army Research Liaison Office Lincoln Laboratory P.O. Box 73 Lexington, Massachusetts
1	USAELRDL Liaison Officer Rome Air Development Center Attn: RAOL Griffiss Air Force Base New York 13442
1	USAEMSA Liaison Office, Far East Signal Office, USARPAC APO 958, U.S. Forces San Francisco, California
1	Technical Director, SELRA/CT Headquarters, USAELRDL
1	USAELRDL Liaison Officer U.S. Army Tank-Automotive Center Warren, Michigan 48090
1	Marine Corps Liaison Office SELRA/LNR, USAELRDL
2	USACDC Liaison Office SELRA/LNF, USAELRDL
1	Commanding Officer U. S. Army Security Agency Processing Center Deal Area - Bldg. 5001
1	Mr. A. H. Young Semiconductor Group Code 681AIA Bureau of Ships Department of the Navy Washington, 25, D. C.
6	Chief, Technical Information Division, Hq, USAELRDL
1	USAELRDL Technical Documents Center SELRA/ADT, Hexagon
1	Director, Electric Components Department, USAELRDL
1	Director, Solid State & Frequency Control Division, EC Department
1	Deputy Director, Solid State & Frequency Control Division, EC Department

DISTRIBUTION LIST (Cont)

No. of Copies	Addressee
1	USAELRDA-White Sands Liaison Office SELRA/LNW, USAELRDL
1	AFSC Scientific/Technical Liaison Office SELRA/LNA, USAELRDL
1	Director, USAEGIMRADA Attn: ENGGM-SS Fort Belvoir, Virginia
5	Chief, Microwave & Quantum Electronics Br., Solid State & Frequency Control Division
1	Chief Scientist U.S. Army Electronics Command Attn: AMSEL-SC Fort Monmouth, New Jersey
1	Commanding General U. S. Army Satellite Communications Agency ATTN: Technical Documents Center Fort Monmouth, New Jersey
5	Chief, Technical Staff, Solid State & Frequency Control Division
5	Chief, Piezoelectric Crystal & Circuitry Br., Solid State & Frequency Control Div.
25	Chief, Semiconductor & Microelectronics Br., Solid State & Frequency Control Div.
1	File Unit Nr.1, Rm 3D-116 Hexagon

Army-Ft Monmouth,NJ-MON 4012-63

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)

Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.

II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.

III. DA Task 1G622001A05602

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)

Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.

II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.

III. DA Task 1G622001A05602

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)

Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.

II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.

III. DA Task 1G622001A05602

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)

Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.

II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.

III. DA Task 1G622001A05602

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of $5x10^4$ ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of $23x10^{-6}$ w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of $5x10^4$ ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of $23x10^{-6}$ w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of $5x10^4$ ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of $23x10^{-6}$ w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of $5x10^4$ ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of $23x10^{-6}$ w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)
Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.
II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.
III. DA Task 1G622001A05602

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)
Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.
II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.
III. DA Task 1G622001A05602

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)
Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.
II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.
III. DA Task 1G622001A05602

AD ________________ Div. ____________

Army Electronics Research and Development Laboratories, Fort Monmouth, N. J.
STATIC AND DYNAMIC PERFORMANCE OF MICRO-POWER TRANSISTOR LINEAR AMPLIFIERS, by R.A. Gilson, O. Pitzalis, W. Kiss and J.D. Meindl, September 1963, 59 p. incl illus., tables, 9 refs. (AELRDL Technical Report 2386 (DA Task 1G622001A05602)
Unclassified Report

Silicon planar transistors which exhibit junction reverse currents smaller than 10^{-9} amperes and common emitter current transfer ratios greater than 50 for collector currents of 10^{-6} amperes are now available. An optimum design technique for the application of these devices in linear broadband amplifiers has been devised. A salient feature of this technique is that it provides a unified approach to the DC and large-signal AC design of a micro-power amplifier. Subject to initial constraints, the design technique: (1)provides a specified amplifier output power capability over a wide temperature range, (2) minimizes amplifier power drain, and

UNCLASSIFIED

1. Micropower Transistor Amplifiers
2. Microelectronic Amplifiers
3. Transistor Amplifiers

I. Gilson, R. A.
Pitzalis, O.
Kiss, W.
Meindl, J. D.
II. Army Electronics Research & Development Laboratories Fort Monmouth, N. J.
III. DA Task 1G622001A05602

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of 5×10^4 ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of 23×10^{-6} w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of 5×10^4 ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of 23×10^{-6} w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of 5×10^4 ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of 23×10^{-6} w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED

(3) maximizes amplifier power gain. With slight modification, the optimum design technique also serves as the basis for a worst case design procedure for linear amplifiers considering transistor and resistor tolerance margins. The frequency response of micropower amplifiers can be accurately predicted on the basis of a unilateralized hybrid pi transistor equivalent circuit. Amplifier bandwidth may be significantly enhanced by means of a cascode circuit. Using a simple thermistor temperature compensation technique, micropower amplifiers have been designed whose gain and terminal impedances are virtually insensitive to large temperature changes.

A common emitter broadband micropower amplifier operating from a three-volt supply with load and source impedances of 5×10^4 ohms can provide a 0.18-v peak AC load voltage over the temperature range $-50 \leq T \leq 100°C$ for a power drain of 23×10^{-6} w and a power gain of 25 db. If the peak load voltage capability is reduced to 0.15 v, this amplifier can accept 10% worst case tolerance margins on all circuit resistors. Depending on transistor barrier capacitances and stray circuit capacitances, amplifier bandwidths vary from about 7 KC to 25 KC with two-to five-time increases possible in the cascode circuit. Further improvements in bandwidth are readily available for larger operating powers.

UNCLASSIFIED